



VELOCITY-4 SATA CFAST™ 7+17 PIN SOLID STATE DRIVE PRODUCT MANUAL

INTERFACE: 3.0 Gb SATA CFAST 7+17 PIN	GENERATION: GEN 1 (1 ST GENERATION)
PART No: V4SDCF-xxU(T)(M)-XXX	MANUAL No: 61000-06652-108
REVISION No: 1.8	REVISION DATE: 10/10/2011

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CONVENTIONS

The following icon and text conventions are used throughout this document to identify additional information of which the reader should be aware.

CONVENTIONS		DESCRIPTION
SHOCK HAZARD		<i>This icon indicates the danger of an electrical shock that may harm or otherwise prove fatal to the user.</i>
CAUTION		This icon indicates the existence of a hazard that could result in equipment or property damage, or equipment failure if the safety instructions are not observed.
ESD		This icon indicates the possible presence of Electrostatic Discharge (ESD or “static electricity”) that may harm the internal electronic components. The user is advised to handle the device only after discharging any possible electrostatic buildup that may be present.
NOTE		This icon identifies information that relates to the safe operation of the equipment or related items.
TIP		This icon identifies helpful hints and tips.
Bold	Text	Used to indicate important technical notes .
<i>Bold Italic</i>	<i>Text</i>	Use to indicate <i>critical instructions</i> .
Light Blue	Text	Used to indicate a hyperlink or “jump” to a related topic or subtopic. The text may be bold .
Dark Blue Bold	Text	Used to indicate a hyperlink or “jump” to a related topic or subtopic. The text may be <i>bold italic</i> .

REVISION HISTORY

REVISION STATUS SUMMARY SHEET			
REVISION	DATE	PAGE(S)	DESCRIPTION
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1.1	04/21/2010	13, 20, 25, 79	Connector Insertion Rating added. Power Consumption Tables combined. ESD Rating changed to TBD.
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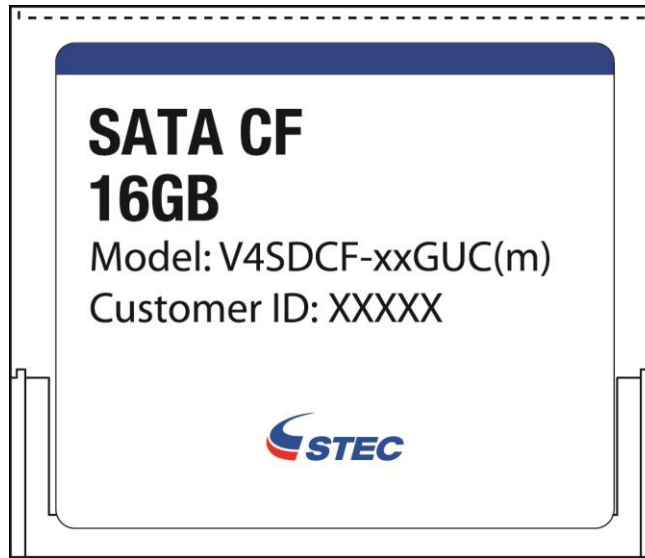


Figure 1: The Velocity-4 CFAST SATA Solid State Drive

OVERVIEW

This document describes the applications, specifications and installation of the Velocity-4 CFAST (CompactFlash ATA Serial Transport) SATA (Serial ATA) Solid State Drive (SSD). See Figure 1.

AUDIENCE

This manual is intended for system engineers or system designers employed by an Original Equipment Manufacturer (OEM). This document was therefore written specifically for a technically advanced audience; it is not intended for end-users that will eventually purchase the commercially available product. The **user**, as referenced throughout the manual, is primarily concerned with industrial, commercial or military computing applications.



This device can be damaged by Electrostatic Discharge (ESD). When handling the device, always wear a grounded wrist strap and use a static dissipative surface.



Any damage to the drive that occurs after its removal from the shipping package and ESD protective trays is the responsibility of the user.

PRODUCT IDENTIFICATION CODES

Table 1 lists the model numbers, unformatted capacities, NAND component type (SLC or MLC NAND) available form factors, and module heights. Each model has a Product Identification Code (Product ID). See the **Part Number Decoder** under **Ordering Information**.

Table 1: Capacities, Form Factors and Case Heights

MODEL NUMBER	CAPACITY	NAND	FORM FACTOR	MODULE HEIGHT
V4SDCF-8UCT-XXX	8GB	SLC	CFAST Type I	≤ 3.6mm
V4SDCF-16UCT-XXX	16GB	SLC	CFAST Type I	≤ 3.6mm
V4SDCF-32UCM-XXX	32GB	MLC	CFAST Type I	≤ 3.6mm

FEATURE OVERVIEW

FEATURE	DESCRIPTION
Form Factor	CFAST Type I
Interface	Serial ATA, SATA 2.6
Connector	
Pin Count	7-Signal, 17-Power and Control
Insertion/Removal Rating	10,000 cycles
Standard Capacities	8, 16, and 32 gigabytes
Custom Capacities	Available upon request.
Operating Voltage	3.3V DC \pm 5%
Temperature	
Commercial	0°C to 70°C
Industrial	N/A
Non-Operating	-25C to 70°C
Interface Bandwidth	3.0 Gb/second
Sequential 128KB Read	100 MB/sec (maximum)
Sequential 128KB Write	60 MB/sec (maximum)
IOPs Random Read – 512 Byte	20,250 IOPs, 4KB Sectors (maximum)
IOPs Random Write – 512 Byte	470 IOPs, 4KB Sectors (maximum)
Wear-Leveling	Dynamic and static algorithms
Bad-Block Management	2% reserve of total flash capacity
Mean Time Between Failures	Two (2) million hours typical MTBF
EDC/ECC	8-bit BCH per 512 bytes
Data Retention	10 years storage
RoHS Compliant	Pb-free components
Warranty	2 years for SLC-based SSDs
	1 year for MLC-based SSDs

STANDARDS AND REFERENCE DOCUMENTS

This section discusses the formal standards that apply to the card. In addition, this section lists the reference documents relevant to the interface protocol used for the card.

COMMERCIAL STANDARDS

The card complies, in whole or in part, with the following commercial standards:

S/NZS 3548 Class B	UL (Underwriters Laboratories)
BSMI CNS 13438 Class B	NEBS Level 3
CAN/CSA-V3/2001.04 (VCCI)	IEC 61000-4-2
CE (Conformite Europeenne)	IEC 61000-4-3
CISPR 22 Class B	IEC 61000-4-4
EN 55022 Class B	IEC 61000-4-5
EN 61000-3-2	IEC 61000-4-6
EN 61000-3-3	IEC 61000-4-8
FCC Part 15 Class B	IEC 61000-4-11

REFERENCE SPECIFICATIONS

The following specifications are relevant to the card:

ORGANIZATION	DOCUMENT	DESCRIPTION
INCITS	T13 1697D	AT Attachment 8 – ATA Serial Transport (ATA8-AST)
INCITS	T13 1699D	AT Attachment 8 – ATA/ATAPI Command Set (ATA-ACS)
INCITS	T13 1510D	Host Adapter Standards (ATA Adapter)
INCTIS	T1 e08108r2	ACS-2 ATA Command Set 2 Project
SATA-IO	2.6	Serial ATA International Organization (SATA-IO) Serial ATA 2.6 Specification, High-Speed Serialized ATA Attachment, February 2007.
Compact Flash Association	CFast 1.0	CFast version 1.0 specification

ELECTROMAGNETIC SUSCEPTIBILITY

The card must be installed in an appropriate enclosure, i.e., a personal computer, host system or alternate enclosure. The user must design the enclosure so that the use of the card does not impair nearby electronic equipment within the same enclosure and external to the enclosure.

The *user*, as defined under the **Audience** section, is responsible for choosing, designing and testing the enclosure so that it is appropriate as previously defined, and complies with relevant regulations, such as Subpart B of Part 15 of FCC Rules and Regulations, and Radio Interference Regulations of the Canadian Department of Communications. Other standards may apply.

ELECTROMAGNETIC COMPATIBILITY

Independent laboratories are in the process of confirming that the card meets the requirements for the CE Mark. While the drive may have CE Marking, the OEM must confirm CE Marking for the product in which the card has been integrated. Test systems confirming the CE Marking may include the following:

CPU Diskette Drive Keyboard Mouse Monitor Printer Modem

MANUFACTURING

LOCATION

Penang, Malaysia

CERTIFICATIONS

ISO 9001 Certified

ISO 14001 Certified

PRODUCT DESCRIPTION

GENERAL DESCRIPTION

The STEC CFAST Type 1 (CFAST) Card is a non-volatile storage device and is intended as a replacement for a hard disk drive (HDD). The card can be configured as a boot or data storage device. The card is Plug and Play compatible; no additional device drivers are required to install the card. The card is recognized by PnP-compatible operating systems and PnP-aware BIOS. The card adheres to the latest industry compliance and regulatory standards, including UL, FCC, RoHS, and the Compact Flash Association (CFA). The rugged industrial design combined with temperature testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments..

SATA INTERFACE

The card can be installed in any system that supports SATA 1.0 or greater devices; the card is compliant with SATA 2 standards and supports all ATA and ATAPI devices. The CFAST card has a fully compliant ATA/ATAPI-8 Serial ATA interface, a 24-pin (7-signal, 17-power/control) connector, and conforms to all the mechanical and mounting requirements for Type I CFAST devices.

DRIVE CAPACITIES

The card is available in unformatted memory capacities of 8, 16, and 32 gigabytes. The memory is comprised of Single-Level Cell (SLC) or Multi-Level Cell (MLC) NAND EEPROM flash components.

PERFORMANCE

The card can operate as sustained read/write transfer rates of up to 138 megabytes per second. Power consumption is kept to a minimum; the card is powered from a 3.3-volt source. The solid state design eliminates electromechanical noise and delay inherent in traditional magnetic rotating media. The wear-leveling and bad-block mapping algorithms ensure data integrity.

PERFORMANCE CHARACTERISTICS

DATA TRANSFER RATES

The data transfer rate of the card is dependent on its flash controller/flash memory configuration. The scalable architecture of the card is capable of minimum sequential and IOPs transfer rates as outlined in Table 2.

Table 2: Data Transfer Rates

TRANSFER RATE	MAXIMUM	UNITS
Interface Bandwidth	3.0	Gb/sec
Sequential Read – 128KB	100	MB/sec
Sequential Write – 128KB	60	MB/sec
IOPs Random Read – 512 Byte	20,250	IOPs, 4KB Sectors
IOPs Random Write – 512 Byte	470	IOPs, 4KB Sectors

ATA MODES

Table 3 lists the ATA operating modes supported by the card.

Table 3: ATA Operating Modes

MODE	SPECIFICATION
PIO	0 – 4
UDMA	0 – 6
Serial ATA	2.6

ENDURANCE

The product life of a SLC-based card is at least two (2) years, and at least one (1) year for a MLC-based card.

WEAR-LEVELING ALGORITHM

The dynamic and static data wear-leveling algorithms integrated in the firmware guarantees that erase/write cycles are evenly distributed across all of the flash memory block locations. Wear-leveling reduces repeated writes to the same physical location.

BAD-BLOCK MANAGEMENT

The bad-block mapping algorithm replaces bad blocks with new ones from available spares. Two percent (2%) of the flash memory is held in reserve (spare blocks) for bad block replacement. Bad blocks in the media are flagged when detected. When any attempt is made to access a flagged block, the selected spare block is substituted. The bad-block mapping function enables data to be automatically transferred from a bad sector to an available spare block.



The drive is scanned for bad blocks during the initialization of the flash components. An initial bad block table is created from these identified marked bad blocks and any bad blocks discovered during the testing process.

DATA RETENTION

This topic is under development.

ERROR DETECTION AND ERROR CORRECTION

The Error Detection Code and Error Correcting Code (EDC/ECC) will maintain data integrity by allowing single or multiple bit corrections to the data stored in the flash array. If the data is corrupted due to aging or during the programming process, EDC/ECC will compensate for the errors to ensure the delivery of accurate data to the host computer. The BCH engine is capable of correcting 8 bits in error per 512 bytes. A retry algorithm is also implemented so that single event disturbances such as ESD or EMF occurring during a read operation can be readily overcome.

RELIABILITY

The following factors affect the reliability statistics:

- DC power is maintained as specified in this document
- Errors caused by the host are excluded from the rates
- Errors from the same causes are counted as 1 block
- Data stream is assumed random

MEAN TIME BETWEEN FAILURES (MTBF)

The average time the card will function without failure is typically two (2) million hours.

ERROR RATES

Table 4 lists the error limit specifications. When all data correction mechanisms are enabled, the error rate will be sustained through all operating temperature ranges as specified in the following sections.

Table 4: Error Limit Specifications

ERROR TYPE	MAXIMUM NUMBER OF ERRORS
Recoverable Data Error	1 bit in 10^{14}
Unrecoverable Data Error	Less than 1 bit in 10^{14}

BUILT-IN SELF-TEST (BIST)

The micro-controller tests the controller memory during power-up, and then performs a back-end status check to verify proper flash memory controller operations. If a fault condition is detected in the flash memory controller, the status of the card is reported as failed.

MOUNT TIME

The time required to initialize and mount the card varies according to the operating system environment and the storage capacity of the drive.

SEEK TIME

The card has no read/write heads or platter. There is no seek time or rotational latency issues. The actual access time may be affected by the operating system and storage capacity of the drive. Mechanical shock, vibration or gravitational forces do not affect transaction throughput, provided the drive is operating within the environmental specifications. See *Environmental Characteristics*.

HOT PLUGGING CARD

The card can be inserted or removed during operation. This capability is known as “hot plugging”. The error recovery procedures will recover from any errors introduced by hot plugging. The method used by the system to detect insertion/removal of the card is dependent upon the scenario. For example, the backplane may be powered, but the card may be in a “quiescent” state. It is recommended that the user reference the Serial ATA 2.6 Specification (Serial ATA International Organization (SATA-IO), High-Speed Serialized ATA Attachment, February 2007) for an overview of the terms and scenarios associated with “hot plugging” serial drives.

Notes:

1. Hot plugging under the SATA 2.0 standard is limited to backplane applications and connections; the card cannot be connected or disconnected for cabled applications.
2. The user should avoid hot plugging a card that has been configured as a boot drive. Unrecoverable errors may be introduced by the operating system if the user attempts to remove a card with an OS installed on it.

REPAIRS

A defective card should be replaced. There are no parts, assemblies or subassemblies that can be repaired by the user. Please see the *Warranty* section on the inside of the back cover page.

Unauthorized repairs to the card will void the warranty.

PREVENTATIVE MAINTENANCE

No preventative maintenance is required. The drive is sealed at the factory, and there are no parts, assemblies or subassemblies that require preventative maintenance on behalf of the user. Please see the *Warranty* section on the inside of the back cover page. ***Unauthorized maintenance to the card will void the warranty.***

ELECTRICAL SPECIFICATIONS

POWER SUPPLY

Table 5 lists the 3.3V DC power specifications for the SSD.

Table 5: 3.3V DC Power Specifications

CONDITION	VALUE	NOTES
Input Voltage	3.30V	±5%
Minimum Voltage	3.14V	Nominal
Maximum Voltage	3.46V	
Ripple	3V, 70mVp-p	±5%
Bulk Capacitance	≤100μF	3V rail
Common Mode Noise Rejection	350mVp-p	100KHz – 200MHz max

POWER CONSUMPTION

The amount of power consumed by the card is determined by the storage (memory) capacity of the drive, and the flash controller/memory configuration of the drive.

Table 6 lists the typical power consumption for the 8GB, 16GB and 32GB cards.

Table 6: 8GB, 16GB, and 32GB Typical Power Consumption

OPERATION	3.3 VOLT	UNIT
Standby/Idle	400	mW
Operating Random Write	0.8	W
Operation Random Read	0.65	W

POWER-ON READY TIME

The Power-On Ready Time is typically ~150ms. It is measured from the time the drive is powered on to the time the drive is ready to accept the first command from the host.

POWER-UP TESTING

The following components are tested for integrity and proper operation during the Power-On cycle:

CPU Check	Reset Drive Registers	Sequencer (FCI) RAM Test
Stack RAM Test	Buffer Scratch Pad RAM	ROM Checksum Verified
Cache RAM Test	Internal RAM Test	Data Path

POWER SAVINGS COMMANDS

The drive will comply with all specifications that define the behavior of storage devices as it relates to power management and Advanced Power Management (APM). When the card receives a power management command, all data in the write cache buffer is written to the media before DRIVE READY is asserted. The card supports the following Power Savings commands and responds with the appropriate status:

Check Power Mode	Idle	Standby	Standby Immediate	Sleep
------------------	------	---------	-------------------	-------

POWER MODE AT POWER ON

The card complies with the latest ATA Power Management Specification. During the Power-On Reset sequence, the drive functions properly and responds as appropriate. In addition, if a SRST (ATA Interface Reset) occurs during this sequence, the drive will respond normally. The drive enters IDLE or STANDBY mode, depending on the setting by the host, after power-on or hard reset.

The card supports with the SATA PHY power modes of PHYRDY, Partial and Slumber. The PHYSLP PHY power mode is optional on CFAST cards and may be supported in future generation cards.

GROUNDING

No special grounding circuitry is required. The host CFAST Card slot should connect to chassis ground with maximum surface contact area to ensure minimal electromagnetic (EM) emissions.

START-UP TIME AND CURRENT DRAW

The Start-Up Time and Current Draw are measured during the power-on phase of the computer and card. See Table 7. The values and current traces reflect the test results of a 32GB unit, but are applicable to all models of the CFAST Card. The measurements were made using a nominal 3.3-volt power supply at room temperature.

Table 7: Start-Up Time and Current Draw

START-UP TIME	300 ms
CURRENT DRAW	
Average RMS	172 mA
Maximum Peak	1.76 A

Figure 2 is the trace for the start-up currents.

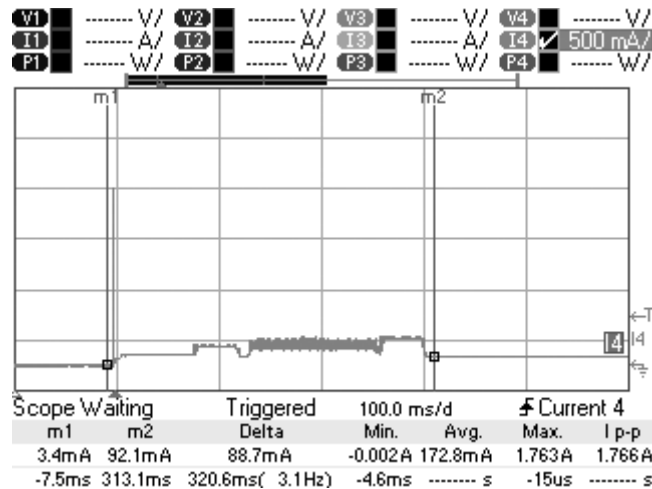


Figure 2: Start-Up Average and Maximum Currents

The timing of the current surge is approximately 735 μ s. See Figure 3.

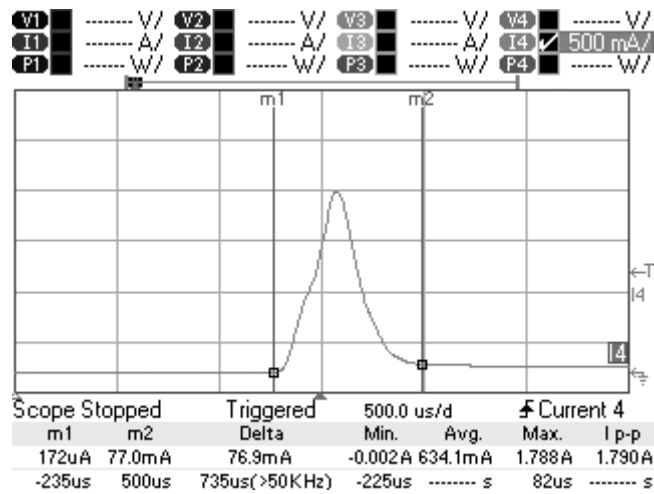


Figure 3: Current Surge Timing

INTERFACE SPECIFICATIONS

CFAST CARD OPERATION

The card is comprised of three primary functional blocks: the interface connector, controller and NAND memory. Read/Write data transfer requests are initiated by the host via the SATA bus interface. Once received, the controller, under the direction of the microcontroller, processes the request.



The microcontroller is responsible for initiating and controlling all activity within the controller, including bad block mapping and executing the wear-leveling algorithms.



The controller decodes an incoming host command, and will configure the appropriate interrupts and status for the local microprocessor to handle various ATA commands. For read and write transfer commands, the hardware can handle the initial handshake with the host automatically. If firmware enables full auto mode, read and write transfers can be fully handled by hardware with minimum firmware support.



Commands that do not require data to be read from or written to the flash memory controller are typically handled by the controller. Some commands may require the controller to use external circuitry that does not involve the flash memory controller.

WRITE OPERATIONS

When a write operation is requested and data is received, the controller uses integrated DMA controllers to transfer the data from host memory to the flash memory controller. The flash memory controller transfers the data from the controller to available locations in the local flash memory of the drive. The controller notifies the host after the write operation is completed.

READ REQUESTS

If a read request is received, the controller retrieves the data from the local flash memory via the flash memory controller. If the controller is responding to a PIO read operation, it presents the data to the ATA bus. If it is responding to a UDMA read request, the controller writes the data directly to system memory on the host. Regardless of the type of operation (PIO or UDMA), the controller notifies the host when the data is ready for transmission.

ACTIVITY LED

Implementation of Pin PC8 (LED1) of the CFAST Card connector is optional. When implemented, this signal is an open drain, 100mA maximum, and can be used with an external LED and series resistor connected to 3.3V. The LED will light during command activity and during periods when the drive indicates a busy state. When not implemented, Pin PC8 is not connected. A second signal, Pin PC9 (LED2) is not connected. See **Power Segment** under **Interface Connector**.

INTERFACE CONNECTOR

The card's SATA connector is divided into a Signal Segment (S1 – S7) and a Power-Control Segment (PC1 – PC17). The card “hot plugs” into a CFAST Card slot as a backplane connection. The connector is designed to blind mate, has staggered contacts to facilitate hot plugging, and supports the future 3.0 Gb/sec speed.

CONNECTOR INSERTION/REMOVAL RATING

The card's connector is rated to be functional after 10,000 insertion/removals cycles as shown in Table 8.

Table 8: Connector Insertion/Removal Cycle Rating

NO. OF INSERTION/REMOVALS	10,000 cycles
----------------------------------	---------------

SIGNAL SEGMENT

SATA uses a protocol transmitted over a 7-pin connection. Figure 4 identifies the 7-pin signal segment. Table 9 lists the signal definitions. The 7-pin signal segment includes 3 grounds, 2 transmit and 2 receive pins. The transmit pins are TxN 5 and TxP 6, and the receive pins are RxP 2 and RxN 3.



*This pin configuration is reversed on the host plug:
Pins 2 and 3 are the transmit pins and 5 and 6 are the receive pins.*



Figure 4: Signal Segment

Table 9: Signal Definitions

PIN	SIGNAL	DESCRIPTION	MATE SEQUENCE
S1	SGND	Signal Ground	1 st Mate
S2	RxP	+ Differential Receive Signal (Phy A)	2 nd Mate
S3	RxN	- Differential Receive Signal (Phy A)	2 nd Mate
S4	SGND	Signal Ground	1 st Mate
S5	TxN	- Differential Transmit Signal (Phy B)	2 nd Mate
S6	TxP	+ Differential Transmit Signal (Phy B)	2 nd Mate
S7	SGND	Signal Ground	1 st Mate

POWER-CONTROL SEGMENT

The power-control segment consists of 17 pins. Figure 5 identifies the 17-pin power-control segment. Table 10 lists the signal definitions.



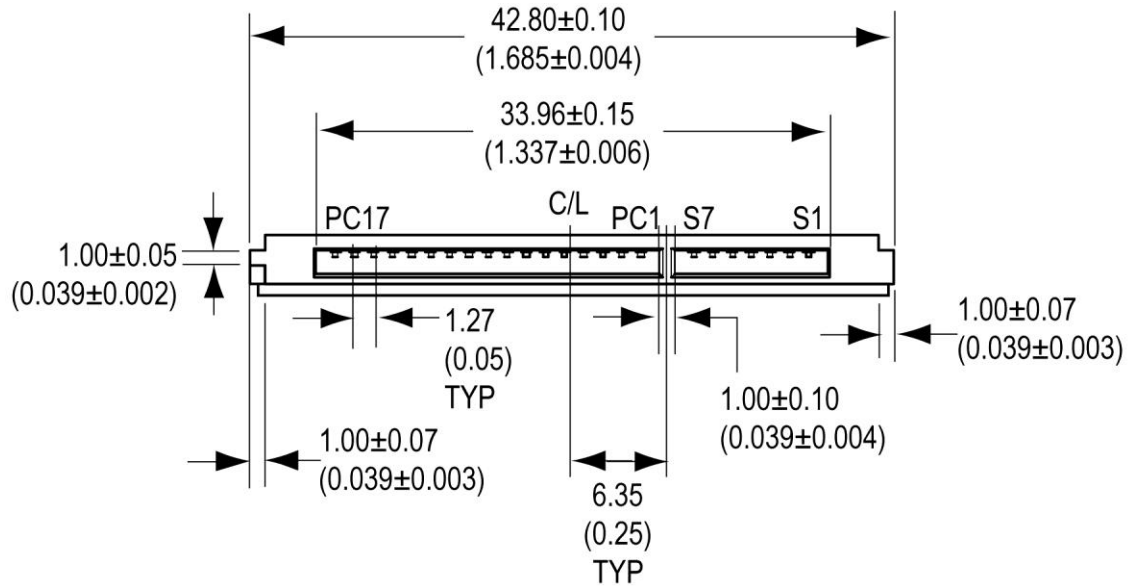
Figure 5: Power-Control Segment

Table 10: Power-Control Definitions

PIN	SIGNAL	DESCRIPTION	MATE SEQUENCE
PC1	CDI	Card Detect In	3 rd Mate
PC2	GND	Device GND	1 st Mate
PC3	-	No Connect	2 nd Mate
PC4	-	No Connect	2 nd Mate
PC5	-	No Connect	2 nd Mate
PC6	-	No Connect	2 nd Mate
PC7	GND	Device Ground	1 st Mate
PC8	LED1	LED Output (Optional)	2 nd Mate
PC9	LED2	LED Output (Not Connected)	2 nd Mate
PC10	IO1	Reserved Input/Output	2 nd Mate
PC11	IO2	Reserved Input/Output	2 nd Mate
PC12	IO3	Reserved Input/Output	2 nd Mate
PC13	VCC	Device Power (3.3V)	2 nd Mate
PC14	VCC	Device Power (3.3V)	2 nd Mate
PC15	PGND	Device Power Ground	1 st Mate
PC16	PGND	Device Power Ground	1 st Mate
PC17	CDO	Card Detect Out	3 rd Mate

CONNECTOR DIMENSIONS

Figure 6 shows the dimension details of the connector. All measurements are in millimeters (inches).



Pin Lengths

First Level		Second Level		Third Level	
Pin	Length	Pin	Length	Pin	Length
S1, S4, S7	0.50±0.10	S2, S34, S5, S6	0.90±0.10	PC1, PC17	1.60±0.10
PC2, PC7	(0.020±0.004)	PC3-PC6	(0.035±0.004)		(0.063±0.004)
PC15, PC16		PC8-PC14			

Figure 6: Connector Dimensions

OVERVIEW

This section summarizes the ATA commands supported by the card. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter and then writing the command code to the register.

COMMAND FLOW

DDMAI0: DMA_in State This state is activated when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command. When in this state, the device shall prepare the data for transfer of a data FIS to the host.

Transition DDMAI0:1 When the device has the data ready to transfer a data FIS, the device shall transition to the DDMAI1: Send_data state.

Transition DDMAI0:2 When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.

DDMAI1: Send_data This state is activated when the device has the data ready to transfer a data FIS to the host. When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2,048 Dwords (8KB).

Transition DDMAI1:1 When the data FIS has been transferred, the device shall transition to the DMAOIO: DMA_in state.

DDMAI2: Send_status This state is activated when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data. When in this state, the device shall request that the Transport layer transmit a Register FIS with the register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.

Transition DDMAI2:1 When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

COMMAND CODES AND REGISTERS

Table 11 lists the commands, command codes and registers accessed by the commands.

Table 11: ATA Command Codes and Registers

COMMAND	IN/OUT/ERROR	REGISTER						
		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
CHECK POWER MODE	Input	98h, E5h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	Yes	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
DEVICE CONFIGURATION RESTORE	Input	B1h	C0	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
DEVICE CONFIGURATION FREEZE LOCK	Input	B1h	C1	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
DEVICE CONFIGURATION IDENTITY	Input	B1h	C2	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
DEVICE CONFIGURATION SET	Input	B1h	C3	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	N/A	Yes	Yes	Yes	Drv/Dev Only
DOWNLOAD MICROCODE	Input	92h	Yes	Yes	Yes	00h	00h	Drv/Dev Only; Hds=0
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
EXECUTE DRIVE DIAGNOSTIC	Input	90h	No	No	No	No	No	No
	Normal Output	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Error Output	No	Yes	No	No	No	No	No
FLUSH CACHE	Input	E7h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes

COMMAND	IN/OUT/ERROR	REGISTER						
		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
FLUSH CACHE EXT	Input	EAh	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Drv/Dev Only
IDENTIFY DEVICE	Input	ECh	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	No	No	No	No	No	No	No
IDLE	Input	97h, E3h	No	Yes	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
IDLE IMMEDIATE	Input	95h, E1h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
INITIALIZE DEVICE PARAMETERS	Input	91h	No	Yes	No	No	No	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
NOP	Input	00h	Yes	No	No	No	No	Drv/Dev Only
	Normal Output	No	No	No	No	No	No	No
	Error Output	Yes	Yes	Yes	Yes	Yes	Yes	Yes
READ BUFFER	Input	E4h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
READ DMA	Input	C8h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
READ DMA EXT	Input	25h	No	Yes	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Drv/Dev Only
READ FPDMA QUEUED	Input	60h	Yes	Yes	Yes	Yes	Yes	Bit 7 (FUA)
	Normal Output	Yes	No	No	No	No	No	No
	Error Output	Yes	Yes	No	No	No	No	No

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COMMAND	IN/OUT/ERROR	REGISTER						
		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
READ LOG EXT	Input	2Fh	No	Yes	Yes	Yes	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
READ MULTIPLE	Input	C4h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
READ MULTIPLE EXT	Input	29h	No	Yes	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Drv/Dev Only
READ NATIVE MAX ADDRESS	Input	F8h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	Yes	Yes	Yes	Yes
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
READ NATIVE MAX ADDRESS EXT	Input	27h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	Yes	Yes	Yes	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
READ SECTOR(S)	Input	20h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
READ VERIFY SECTOR(S)	Input	40h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
SECURITY DISABLE PASSWORD	Input	F6h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SECURITY ERASE PREPARE	Input	F3h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SECURITY ERASE UNIT	Input	F4h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only

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		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
SECURITY FREEZE LOCK	Input	F5h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SECURITY SET PASSWORD	Input	F1h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SECURITY UNLOCK	Input	F2h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SEEK	Input	70h	No	No	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET FEATURES	Input	EFh	Subcommand Specific					Drv/Dev Only
	Normal Output							
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MAX ADDRESS	Input	F9h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	Yes	Yes	Yes	Yes
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MAX FREEZE LOCK	Input	F9h	04h	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MAX LOCK	Input	F9h	02h	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MAX SET PASSWORD	Input	F9h	01h	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MAX UNLOCK	Input	F9h	03h	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only

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COMMAND	IN/OUT/ERROR	REGISTER						
		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
SET MAX ADDRESS EXT	Input	37h	No	No	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	Yes	Yes	Yes	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SET MULTIPLE MODE	Input	C6h	No	Yes	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SLEEP	Input	E6h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART READ DATA	Input	B0h	D0h	No	No	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART ENABLE/ DISABLE ATTRIBUTE AUTOSAVE	Input	B0h	D2h	00h/F1h	No	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART EXECUTE OFF-LINE IMMEDIATE	Input	B0h	D4h	No	Yes	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	N/A or 4Fh	N/A or C2h	Drv/Dev Only
	Error Output	Yes	Yes	No	No	N/A, 4Fh, or F4h	N/A, C2h, or 2Ch	Drv/Dev Only
SMART READ LOG	Input	B0h	D5h	Yes	Yes	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART WRITE LOG	Input	B0h	D6h	Yes	Yes	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART ENABLE OPERATIONS	Input	B0h	D8h	No	No	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
SMART DISABLE OPRERATIONS	Input	B0h	D9h	No	No	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only

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COMMAND	IN/OUT/ERROR	REGISTER						
		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
SMART RETURN STATUS	Input	B0h	DAh	No	No	4Fh	C2h	Drv/Dev Only
	Normal Output	Yes	No	No	No	4Fh or F4h	C2h or 2Ch	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
STANDBY	Input	96h, E2h	No	Yes	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
STANDBY IMMEDIATE	Input	94h, E0h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
WRITE BUFFER	Input	E8h	No	No	No	No	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
WRITE DMA	Input	CAh	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
WRITE DMA EXT	Input	35h	No	Yes	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
WRITE FPDMA QUEUED	Input	61h	Yes	Yes	Yes	Yes	Yes	Bit 7 (FUA)
	Normal Output	Yes	No	No	No	No	No	No
	Error Output	Yes	Yes	No	No	No	No	No
WRITE LOG EXT	Input	3Fh	No	Yes	Yes	Yes	No	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	No	No	No	Drv/Dev Only
WRITE MULTIPLE	Input	C5h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
WRITE MULTIPLE EXT	Input	39h	No	Yes	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Drv/Dev Only

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		COMMAND STATUS	FEATURE ERROR	SECTOR COUNT	SECTOR LBA LOW	CYLINDER LOW LBA MID	CYLINDER HIGH LBA HIGH	DRIVE/HEAD DEVICE/LBA
WRITE SECTOR(S)	Input	30h	No	Yes	Yes	Yes	Yes	Yes
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Yes
WRITE SECTOR(S) EXTENDED	Input	34h	No	Yes	Yes	Yes	Yes	Drv/Dev Only
	Normal Output	Yes	No	No	No	No	No	Drv/Dev Only
	Error Output	Yes	Yes	No	Yes	Yes	Yes	Drv/Dev Only

COMMAND SUMMARY

Table 12 provides a summary of each supported ATA command.

Table 12: ATA Command Summary

COMMAND	HEX VALUE	DESCRIPTION
CHECK POWER MODE	98h, E5h	This command allows the host to determine the current power mode of the device. The command shall not cause the device to change power or affect the operation of the Standby timer.
DEVICE CONFIGURATION FREEZE LOCK	B1h, C1h	This 28-bit command is mandatory for devices that implement the DCO feature set. The command allows the host to prevent any accidental modification of the DCO settings. If the device completes the command without error, it will abort any subsequent DCO commands until the device processes a power-on reset. A device shall be in the <i>factory_config</i> or <i>reduced_config</i> state after processing a power-on reset. The device shall not exit the <i>DCO_Locked</i> state as the result of processing a hardware reset or software reset.
DEVICE CONFIGURATION IDENTIFY	B1h, C2h	This 28-bit command is mandatory for devices that implement the DCO feature set. The command will cause a device to return a 512-byte data structure. The content of the structure will indicate the commands, modes and feature sets the device can select and modify through the processing of a DEVICE CONFIGURATION SET command.
DEVICE CONFIGURATION RESTORE	B1h, C3h	This 28-bit command is mandatory for devices that implement the DCO feature set. The command allows the host to restore any setting that was previously modified using a DEVICE CONFIGURATION SET command and restore the content of the IDENTIFY DEVICE data and other feature settings to the factory default values.
DEVICE CONFIGURATION SET	B1h, C3h	This 28-bit command is mandatory for devices that implement the DCO feature set. The command allows the host to reduce the set of optional commands, modes or feature sets supported by a device as indicated by the DEVICE CONFIGURATION IDENTIFY command. The command may modify the data returned by the IDENTIFY DEVICE (ECh) command; the device shall respond in a manner consistent with the new data.
DOWNLOAD MICROCODE	92h	This command allows the host to alter the microcode of the device. The data transferred using the Download Microcode command is vendor-specific. All transfers are an integer multiple of the sector size. The size of the data transfer is determined by the contents of the LBA Low register and the Sector Count register. The LBA Low register will extend the Sector Count register to create a 16-bit sector count value. The LBA Low register will be the most significant eight bits and the Sector Count register will be the least significant eight bits. A value of zero in the LBA Low and Sector Count registers specify that no data is to be transferred. This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512-byte increments. The Features register will determine the effect of the Download Microcode command.

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COMMAND	HEX VALUE	DESCRIPTION
EXECUTE DRIVE DIAGNOSTIC	90h	This command performs the internal diagnostic tests implemented by the controller.
FLUSH CACHE	E7h	This command is used by the host to request that the device flush the Write cache. If there is data in the cache, that data shall be written to the media. The command will not indicate completion until the data is flushed to the media or an error occurs. If the device supports more than 28 bits of addressing, this command shall attempt to flush all the data in the cache. If the cache is disabled or is not present, the device will indicate completion without error. The command is mandatory for devices not implementing the Packet feature set.
FLUSH CACHE EXT	EAh	This command is used by the host to request that the device flush the Write cache. If there is data in the cache, that data shall be written to the media. The command will not indicate completion until the data is flushed to the media or an error occurs. If the cache is disabled or is not present, the device will indicate completion without error. This command is mandatory for devices that implement the 48-bit Address feature set.
IDENTIFY DEVICE	ECh	This command allows the host to receive parameter information from the drive.
IDLE	97h, E3h	This command will cause the drive to set BSY, enter the IDLE mode, clear BSY, and generate an interrupt. If the sector count is zero, the automatic power down mode is disabled.
IDLE IMMEDIATE	95h, E1h	This command will cause the drive to set BSY, enter the IDLE (READ) mode, clear BSY, and generate an interrupt.
INITIALIZE DEVICE PARAMETERS	91h	This command will enable the host to set the number of sectors per track and the number of heads per cylinder.
NOP	00h	This command is mandatory for devices that implement the Packet and TCQ feature sets. The device will respond with command aborted. For devices that implement the TCQ feature set, the subcommand 00h in the Feature field shall abort any outstanding queue. Subcommand codes 01h through FFh in the Feature field shall not affect the status of any outstanding queue.
READ BUFFER	E4h	This command is optional for devices that do not implement the Packet feature set. The command will enable the host to read a 512-byte block of data. The Write Buffer (E8h) command should precede the Read Buffer (E4h) command, lest the data returned be indeterminate.
READ DMA	C8h	This command is mandatory for devices that do not implement the Packet feature set. The command will allow the host to read data using the DMA data transfer protocol.

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COMMAND	HEX VALUE	DESCRIPTION
READ DMA EXT	25h	This command is mandatory for devices that implement the 48-bit Address feature set. The command will allow the host to read data using the DMA data transfer protocol.
READ FPDMA QUEUED	60h	This 48-bit command is mandatory for devices that implement the NCQ feature set. The command will transfer data from the device to the host. If the FUA (Forced Unit Access) bit is set to one (1), the device shall retrieve the data from the non-volatile media regardless of whether the requested data is in the volatile media. If the device holds a modified copy of the requested data as a result of multiple cached writes, the modified data shall be written to the non-volatile media before being retrieved from the non-volatile media. When the FUA bit is cleared to zero (0), the data can be retrieved from either the non-volatile media or cache.
READ LOG EXT	2Fh	This 48-bit command is mandatory for devices that implement the GPL feature set. The command returns the specified log to the host.
READ MULTIPLE	C4h	This command is similar to the Read Sector(s) - 20h command. Interrupts are not generated on each sector, but on the transfer of a block that contains the number of sectors as defined by a Set Multiple Mode - C6h command.
READ MULTIPLE EXT	29h	This command is mandatory for all devices that implement the 48-bit Address feature set. The command will read the number of logical sectors specified in the Count field. The number of logical sectors determines the DRQ data block count, which in turn will determine the number of logical sectors that are to be transferred.
READ NATIVE MAX ADDRESS	F8h	This command is mandatory for devices that implement the 28-bit HPA feature set. The command will return the native max address; the maximum LBA that is valid when using the SET MAX ADDRESS command. If the 48-bit Address feature set is supported, and the 48-bit native max address is greater than 268,435,455, the READ NATIVE MAX ADDRESS command will return the same maximum value.
READ NATIVE MAX ADDRESS EXT	27h	This command is mandatory for devices that implement the 48-bit HPA feature set and 48-bit Address feature set. The command will return the native max address; the maximum LBA that is valid when using the SET MAX ADDRESS EXT command.
READ SECTOR(S)	20h	This command will read from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 (zero) requests 256 sectors. The transfer will begin at the sector specified in the Sector Number Register.

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COMMAND	HEX VALUE	DESCRIPTION
READ SECTOR(S) EXT	24h	This command is mandatory for devices that implement the 48-bit Address feature set. This command will read from 1 to 256 to 65,536 logical sectors as specified in the Sector Count Register. A sector count of 0 (zero) will request 65,536 logical sectors. The transfer will begin at the sector specified in the LBA field.
READ VERIFY SECTOR(S)	40h	This command will verify one or more sectors by transferring data from the flash media to the data buffer and verifying that the ECC is correct. The command is identical to the Read Sector(s) - 20h command, except that DRQ is never set and no data is transferred to the host.
READ VERIFY SECTOR(S) EXT	42h	This command is mandatory for devices that implement the 48-bit Address feature set. The command is identical to the Read Sector(s) Extended (24) command, except that no data is transferred from the device to the host. The device will read the data stored in the media and verify that no errors exist.
SECURITY DISABLE PASSWORD	F6h	This command is mandatory for devices that implement the Security Mode feature set. The command will transfer 512 bytes of predefined data from the host. If the password selected by Word 0 matches the password that was previously saved by the device, the device shall disable Lock mode. The command will not change the Master password. The Master password is reactivated when a User password is set. The command will only complete successfully if the device is in Unlocked mode.
SECURITY ERASE PREPARE	F3h	This command is mandatory for devices that implement the Security Mode feature set. The command is issued immediately before the Security Erase Unit (F4h) command to enable device erasing and unlocking. The command prevents accidental loss of data on the device.
SECURITY ERASE UNIT	F4h	This command is mandatory for devices that implement the Security Mode feature set. The command will transfer 512 bytes of predefined data from the host. If the password does not match the password previously saved by the device, the device shall reject the command and abort it. When a Normal Erase mode is specified, the Security Erase Unit command shall write binary zeros to all user data areas. If the optional Enhanced Erase mode is specified, the device shall write predetermined data patterns to all user data areas; the current data is overwritten, including sectors that are no longer in use due to reallocation.
SECURITY FREEZE LOCK	F5h	This command is mandatory for devices that implement the Security Mode feature set. The command shall set the device to Frozen mode. Other commands that update the device Lock mode are aborted. Frozen mode can be disabled by a power-off or hardware reset. If the command is issued while the device is in Frozen mode, the command is executed and the device will remain in Frozen mode.

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COMMAND	HEX VALUE	DESCRIPTION
SECURITY SET PASSWORD	F1h	This command is mandatory for devices that implement the Security Mode feature set. The command will transfer 512 bytes of predefined data from the host. The data controls the function of this command, which in turn defines the interaction of the identifier and security level bits. The user can in turn set the Master or User passwords, and the security level of the device.
SECURITY UNLOCK	F2h	This command is mandatory for devices that implement the Security Mode feature set. The command will transfer 512 bytes of predefined data from the host. The data controls the function of this command, which in turn defines the interaction of the Identifier bit. If the Identifier bit is set to Master and the current security level is high, the password is compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected. If the Identifier bit is set to User, then the device shall compare the supplied password with the stored User password. If the password comparison fails, the device shall abort the command and report a decrease in the incremental value in the unlock counter.
SEEK	70h, 7Fh	This command is effectively a NOP command to the SSD although it does perform a range check.
SET FEATURES	EFh	This command is used by the host to establish or select certain features supported by the drive. When the SSD receives this command, it sets BSY, checks the contents of the Features register, applies changes as necessary, clears BSY and generates an interrupt. If the value in the register does not represent a feature supported by the drive, the command is canceled with the Abort Error condition.
SET MAX	-	Each SET MAX command is identified by the value placed in the <i>Feature</i> field.
SET MAX ADDRESS	F9h	This 28-bit command is mandatory for devices that implement the HPA feature set. The command will reject all read/write access attempts to an LBA that is greater than the specified LBA set by the command. If an attempt is made to read/write to an LBA greater than that specified by SET MAX ADDRESS, then the ID Not Found bit is set to one and the ID Not Found error is reported. The IDENTIFY DEVICE data words 60-61 will reflect the maximum LBA set using this command.
SET MAX FREEZE LOCK	F9h, 04h	This 28-bit command is mandatory for devices that implement the HPA Security Extensions. The command will disable the following commands: SET MAX ADDRESS, SET MAX SET PASSWORD, SET MAX LOCK, SET MAX UNLOCK and SET MAX ADDRESS EXT. Any subsequent SET MAX commands will be aborted until the device processes a power-on reset.

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COMMAND	HEX VALUE	DESCRIPTION
SET MAX LOCK	F9h, 02h	This 28-bit command is mandatory for devices that implement the HPA Security Extensions. A device will be "HPA Locked" after successful execution of the command; the HPA Security Extensions unlock counter is set to a value of five (5). Any subsequent SET MAX commands, except SET MAX UNLOCK and SET MAX FREEZE LOCK, shall be aborted. The device will remain in the "locked" state until a power-on reset or the successful completion of the SET MAX UNLOCK or SET MAX FREEZE LOCK commands.
SET MAX SET PASSWORD	F9h, 01h	This 28-bit command is mandatory for devices that implement the HPA Security Extensions. The command will request a transfer of a single 512-byte block from the host. The password is not retained after the device processes a power-on reset.
SET MAX UNLOCK	F9h, 03h	This 28-bit command is mandatory for devices that implement the HPA Security Extensions. The command will request a transfer of a single 512-byte block from the host. The password contained within the data transfer is compared with the password set with the SET MAX SET PASSWORD command.
SET MAX ADDRESS EXT	37h	This 48-bit command is similar to SET MAX ADDRESS, but is for devices that implement both the HPA feature set and 48-bit Address feature set. The command will reject all read/write access to an LBA that is greater than the specified LBA set by the command. If an attempt is made to read/write to an LBA greater than that specified by SET MAX ADDRESS EXT, then the ID Not Found bit is set to one and the ID Not Found error is reported. The IDENTIFY DEVICE data and maximum LBA remain unchanged should SET MAX ADDRESS EXT fail.
SET MULTIPLE MODE	C6h	This command enables the SSD to perform multiple read and write operations and establishes the block count for these commands.
SLEEP	E6h	This command is mandatory for devices that implement the Power Management feature set. The command will cause the device to enter Sleep mode. The device will not power-on in Sleep mode nor remain in the mode following a reset sequence. The method used to deactivate Sleep mode is transport specific. The Power Management feature set is mandatory for devices that do not implement the Packet Command set. This command is mandatory when power management is not implemented by the PACKET Command set device.
SMART	B0h, Dxh	See <i>S.M.A.R.T. Specification</i> .
STANDBY	96h, E2h	This command will configure the drive for Standby Mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the drive returns to Idle Mode, the timer starts a countdown. The time is set in the Sector Count Register.
STANDBY IMMEDIATE	94h, E0h	This command will cause the SSD to set BYS, enter the Standby Mode, clear BSY, and return the interrupt immediately.

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COMMAND	HEX VALUE	DESCRIPTION
WRITE BUFFER	E8h	This command is optional for devices that implement the General feature set. This command allows the host to write the contents of one 512-byte block of data in the in the buffer of the device.
WRITE DMA	CAh	This command is mandatory for devices that implement the General feature set. The command allows the host to write data using the DMA data transfer protocol.
WRITE DMA EXT	35h	This command is mandatory for devices that implement the 48-bit Address feature set. The command allows the host to write data using the DMA data transfer protocol.
WRITE FPDMA QUEUED	61h	This command is mandatory for devices that implement the 48-bit NCQ feature set. The command will transfer data from the host to the device. If the FUA (Forced Unit Access) bit is set to one (1), regardless of whether volatile/non-volatile write caching is enabled, the user data shall be written to non-volatile media before command completion is reported. When the FUA bit is cleared to zero, the device may return command completion before the data is written to the non-volatile media.
WRITE LOG EXT	3Fh	This 48-bit command is mandatory for devices that implement the General Purpose Logging feature set. The command will write a specified number of 512-byte blocks of data to the specified log.
WRITE MULTIPLE	C5h	This command is similar to the Write Sector(s) - 30h command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by the Set Multiple Mode - C6h command.
WRITE MULTIPLE EXT	39h	This command is mandatory for devices that implement the 48-bit Address feature set. The command will write the number of logical sectors specified in the Count field. The command is similar to Write Sector(s) (30h). Interrupts are not presented on each sector, but on the transfer of blocks that contain the number of sectors defined by LBA mode.
WRITE SECTOR(S)	30h	This command will write from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 (zero) will request 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
WRITE SECTOR(S) EXT	34h	This command is mandatory for devices that implement the 48-bit Address feature set. The command will write 1 to 65,536 logical sectors as specified in the Sector Count Register. A sector count value of 0 will request 65,536 logical sectors.


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IDENTIFY DEVICE (ECh) OVERVIEW

The IDENTIFY DEVICE (ECh) command enables the host to receive parameter information from the card. When the command executes, the SSD sets the BSY bit, prepares to transfer the 256 words of card identification data to the host, sets the DRQ bit, clears the BSY bit, and then generates an interrupt. The host can then transfer the data by reading the data register. All reserved bits or words are all zero.

IDENTIFY DEVICE (ECh) INFORMATION KEY	
DESIGNATORS	DESCRIPTION
O/M	Optional/Mandatory Requirement <ul style="list-style-type: none"> O Support of the word is optional. M Support of the word is mandatory.
S/P	Serial or Parallel Transport <ul style="list-style-type: none"> S Serial Transport P Parallel Transport B Both Serial and Parallel Transports N Belongs to a transport other than Serial or Parallel.
F/V	Fixed/Variable Content <ul style="list-style-type: none"> F The content of the word is fixed and does not change. For removable media devices, these values may change when the media is removed or changed. The DCO command may change the value of a fixed field. V The content of the word is variable and may change according to the state of the device or the command executed by the device. X The content of the word is vendor-specific and may be fixed or variable. R The content of the word is reserved and shall be 0 (zero).
	It is recommended that the user reference <i>INCITS T13/1699-D, Information Technology – ATA Attachment 8 – ATA ATAPI Command Set (ATA9-ACS), Revision 6a, September 6, 2008</i> for details.

IDENTIFY DEVICE (ECh) DATA FORMAT

Table 13 specifies the format of the IDENTIFY DEVICE (ECh) data.

Table 13: IDENTIFY DEVICE Data Format

WORD	O/M	S/P	F/V	DESCRIPTION
0	M	B		General Configuration
			F	15 0 = ATA Device
			X	14:8 Retired
			X	7:6 Obsolete
			X	5:3 Retired
			V	2 Response Incomplete
			X	1 Retired
				0 Reserved
1			X	Obsolete
2	O	B	V	Specific Configuration
3			X	Obsolete
4-5			X	Retired
6			X	Obsolete
7-8		N		Reserved for the CompactFlash Association
9			X	Retired
10-19	M	B	F	Serial Number (ATA String)
20-21			X	Retired
22			X	Obsolete
23-26	M	B	F	Firmware Revision (ATA String)
27-46	M	B	F	Model Number (ATA String)
47	M			
		B	F	15:8 80h
		B	F	7:0 00h = Reserved
				01h- FFh = Maximum number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands.

48	O	B	F	Trusted Computing Feature Set Options
			F	15 Shall be cleared to zero.
			F	14 Shall be set to one.
			13:1	Reserved for the Trusted Computing Group.
			F	0 1 = Trusted Computing Feature Set is supported.
49	M			Capabilities
		B	F	15:14 Reserved for the IDENTIFY PACKET DEVICE command.
			F	13 1 = Standby timer values as specified in this standard are supported.
				0 = Standby timer values shall be managed by the device.
		P	F	12 Reserved for the IDENTIFY PACKET DEVICE command.
			F	11 1 = IORDY supported.
				0 = IORDY may be supported.
		P	F	10 1 = IORDY may be disabled.
		B	F	9 Shall be set to one to indicate that LBA is supported.
		P	F	8 1 = DMA supported.
			X	7:0 Retired
50	M			Capabilities
		B	F	15 Shall be cleared to zero.
		B	F	14 Shall be set to one.
				13:2 Reserved
			X	1 Obsolete
		B	F	0 Shall be set to one to indicate a vendor-specific Standby Timer Value minimum.
51-52			X	Obsolete
53	M	B	F	15:8 Free-Fall Control Sensitivity
				00h = Recommended vendor setting.
				01h-FFh = Sensitivity Level. The greater the value, the more sensitive the setting.
				7:3 Reserved

		B	F	2	1 = The fields reported in Word 88 are valid. 0 = The fields reported in Word 88 are not valid.
		B	F	1	1 = The fields reported in Words (70:64) are valid. 0 = The fields reported in Words (70:64) are not valid.
			X	0	Obsolete
54-58			X		Obsolete
59	M	B	V	15:9	Reserved
		B	V	8	1 = Multiple Sector Setting is valid.
		B	V	7:0	Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands.
60-61	M	B	F		Total Number of User-Addressable Logical Sectors for 28-bit commands (DWord).
62			X		Obsolete
63	M	P	V	15:11	Reserved
		P	V	10	1 = Multiword DMA Mode 2 is selected. 0 = Multiword DMA Mode 2 is not selected.
		P	V	9	1 = Multiword DMA Mode 1 is selected. 0 = Multiword DMA Mode 1 is not selected.
		P	V	8	1 = Multiword DMA Mode 0 is selected. 0 = Multiword DMA Mode 0 is not selected.
				7:3	Reserved
		P	F	2	1 = Multiword DMA Mode 2 and below are supported.
		P	F	1	1 = Multiword DMA Mode 1 and below are supported.
		P	F	0	1 = Multiword DMA Mode 0 is supported.
64	M	P	F	15:8	Reserved
				7:0	PIO Modes supported.
65	M	P	F		Minimum Multiword DMA Transfer Cycle Time per Word
				15:0	Cycle Time in nanoseconds.

66	M			Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15:0 Cycle Time in Nanoseconds.
		P	F	
67	M			Minimum PIO Transfer Cycle Time without Flow Control 15:0 Cycle Time in nanoseconds.
		P	F	
68	M			Minimum PIO Transfer Cycle Time with IORDY Flow Control 15:0 Cycle Time in nanoseconds.
		P	F	
69-70				Reserved
71-74				Reserved for the IDENTIFY PACKET DEVICE command.
75	O			Queue Depth 15:5 Reserved 4:0 Maximum Queue Depth - 1
		B	F	
76	O	S		Serial ATA Capabilities 15:11 Reserved for Serial ATA 10 1 = Supports PHY Event Counters 9 1 = Supports receipt of host-initiated power management requests. 8 1 = Supports the NCQ Feature Set 7:3 Reserved for Serial ATA 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s). 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s). 0 Shall be cleared to zero.
			F	
			F	
			F	
			F	
			F	
			F	
77				Reserved for Serial ATA
78	O	S		Serial ATA Features Supported 15:7 Reserved for Serial ATA 6 1 = Device supports Software Settings Preservation. 5 Reserved for Serial ATA 4 1 = Device supports In-Order Data Delivery. 3 1 = Device supports Initiating Power Management. 2 1 = Device supports DMA Setup Auto-Activation.
			F	
			F	
			F	
			F	

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			F	1 1 = Device supports Non-Zero Buffer Offsets.
			F	0 Shall be cleared to zero.
79	O	S		Serial ATA Features Enabled
				15:7 Reserved for Serial ATA
			V	6 1 = Software Settings Preservation enabled.
				5 Reserved for Serial ATA
			V	4 1 = In-Order Data Delivery enabled.
			V	3 1 = Device Initiated Power Management enabled.
			V	2 1 = DMA Setup Auto-Activation enabled.
			V	1 1 = Non-Zero Buffer Offsets enabled.
			F	0 Shall be cleared to zero.
80	M			Major Version Number
				15:9 Reserved
		B	F	8 1 = Supports ATA8-ACS.
		B	F	7 1 = Supports ATA/ATAPI-7.
		B	F	6 1 = Supports ATA/ATAPI-6.
		B	F	5 1 = Supports ATA/ATAPI-5.
		B	F	4 1 = Supports ATA/ATAPI-4.
			X	3 Obsolete
			X	2 Obsolete
			X	1 Obsolete
				0 Reserved
81	M	B	F	Minor Version Number
82	M			Commands and Feature Sets Supported
			X	15 Obsolete
		B	F	14 1 = The NOP command is supported.
		B	F	13 1 = The READ BUFFER command is supported.
		B	F	12 1 = The WRITE BUFFER command is supported.

		X	11	Obsolete
		B	F	10 1 = The HPA Feature Set is supported.
		B	F	9 Shall be cleared to zero to indicate that the DEVICE RESET command is not supported.
		B	F	8 1 = The SERVICE Interrupt is supported.
		B	F	7 1 = The RELEASE Interrupt is supported.
		B	F	6 1 = Read Look-Ahead is supported.
		B	F	5 1 = The Volatile Write Cache is supported.
		B	F	4 Shall be cleared to zero to indicate that the PACKET Feature Set is not supported.
		B	F	3 Shall be set to one to indicate that the mandatory Power Management Feature Set is supported.
			X	2 Obsolete
		B	F	1 1 = The Security Feature Set is supported.
		B	F	0 1 = The SMART Feature Set is supported.
83	M			Commands and Feature Sets Supported
			F	15 Shall be cleared to zero.
			F	14 Shall be set to one.
		B	F	13 1 = The FLUSH CACHE EXT command is supported.
		B	F	12 Shall be set to one to indicate that the mandatory FLUSH CACHE command is supported.
		B	F	11 1 = The DCO Feature Set is supported.
		B	F	10 1 = The 48-Bit Address Feature Set is supported.
		B	F	9 1 = The AAM Feature Set is supported.
		B	F	8 1 = The SET MAX security extension is supported.
				7 Reserved for the Address Offset Reserved Area Boot Method
		B	F	6 1 = SET FEATURES subcommand is required to spin-up after power-up.
		B	F	5 1 = The PUIS Feature Set is supported.
			X	4 Obsolete
		B	F	3 1 = The APM Feature Set is supported.

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		N	F	2	1 = The CFA Feature Set is supported.
		B	F	1	1 = The TCQ Feature Set is supported.
		B	F	0	1 = The DOWNLOAD MICROCODE command is supported.
84	M			Commands and Feature Sets Supported	
			F	15	Shall be cleared to zero.
			F	14	Shall be set to one.
		B	F	13	1 = The IDLE IMMEDIATE command with UNLOAD feature is supported.
				12	Reserved for TLC.
				11	Reserved for TLC.
			X	10:9	Obsolete
		B	F	8	1 = The 64-Bit World Wide Name is supported.
		B	F	7	1 = The WRITE DMA QUEUED FUA EXT command is supported.
		B	F	6	1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported.
		B	F	5	1 = The GPL Feature Set is supported.
		B	F	4	1 = The Streaming Feature Set is supported.
		N	F	3	1 = The Media Card Pass Through Command Feature Set is supported.
		B	F	2	1 = Media Serial Number is supported.
		B	F	1	1 = The SMART Self-Test is supported.
		B	F	0	1 = SMART Error Logging is supported.
85	M			Commands and Feature Sets Supported or Enabled	
			X	15	Obsolete
		B	F	14	1 = The NOP command is supported.
		B	F	13	1 = The READ BUFFER command is supported.
		B	F	12	1 = The WRITE BUFFER command is supported.
			X	11	Obsolete
		B	V	10	1 = HPA Feature Set is supported.

		B	F	9 Shall be cleared to zero to indicate that the DEVICE RESET command is not supported.
		B	V	8 1 = The SERVICE interrupt is enabled.
		B	V	7 1 = The RELEASE interrupt is enabled.
		B	V	6 1 = Read Look-Ahead is enabled.
		B	V	5 1 = The volatile write cache is enabled.
		B	F	4 Shall be cleared to zero to indicate that the PACKET Feature Set is not supported.
		B	F	3 Shall be set to one to indicate that the mandatory Power Management Feature Set is supported.
			X	2 Obsolete
		B	V	1 1 = The Security Feature Set is enabled.
		B	V	0 1 = The SMART Feature Set is enabled.
86	M	B	F	15 1 = Words 119-120 are valid.
				14 Reserved
		B	F	13 1 = FLUSH CACHE EXT command supported.
		B	F	12 1 = FLUSH CACHE command supported.
		B	F	11 1 = The DCO Feature Set is supported.
		B	F	10 1 = The 48-Bit Address Feature Set is supported.
		B	V	9 1 = The AMM Feature Set is enabled.
		B	V	8 1 = The SET MAX security extension is enabled by SET MAX SET PASSWORD.
				7 Reserved for Address Offset Reserved Area Boot Method.
		B	V	6 1 = SET FEATURES subcommand is required to spin-up after power-up.
		B	V	5 1 = The PUIS Feature Set is enabled.
			X	4 Obsolete
		B	V	3 1 = The APM Feature Set is supported.
		N	F	2 1 = The CFA Feature Set is supported.
		B	F	1 1 = The TCQ Feature Set is supported.
		B	F	0 1 = The DOWNLOAD MICROCODE command is supported.
Commands and Feature Sets Supported or Enabled				

87	M			<p>Commands and Feature Sets Supported or Enabled</p> <p>F 15 Shall be cleared to zero.</p> <p>F 14 Shall be set to one.</p> <p>B F 13 1 = The IDLE IMMEDIATE command with UNLOAD FEATURE is supported.</p> <p>12 Reserved for TLC.</p> <p>11 Reserved for TLC.</p> <p>X 10:9 Obsolete</p> <p>B F 8 1 = The 64-Bit World Wide Name is supported.</p> <p>B F 7 1 = The WRITE DMA QUEUED FUA EXT command is supported.</p> <p>B F 6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported.</p> <p>B F 5 1 = The GPL Feature Set is supported.</p> <p>X 4 Obsolete</p> <p>N V 3 1 = The Media Card Pass Through Command Feature Set is supported.</p> <p>B V 2 1 = Media Serial Number is valid.</p> <p>B F 1 1 = SMART Self-Test supported.</p> <p>B F 0 1 = SMART Error Logging is supported.</p>
88	O			<p>Ultra DMA Modes</p> <p>15 Reserved</p> <p>P V 14 1 = Ultra DMA Mode 6 is selected.</p> <p>0 = Ultra DMA Mode 6 is not selected.</p> <p>P V 13 1 = Ultra DMA Mode 5 is selected.</p> <p>0 = Ultra DMA Mode 5 is not selected.</p> <p>P V 12 1 = Ultra DMA Mode 4 is selected.</p> <p>0 = Ultra DMA Mode 4 is not selected.</p> <p>P V 11 1 = Ultra DMA Mode 3 is selected.</p> <p>0 = Ultra DMA Mode 3 is not selected.</p>

		P	V	10	1 = Ultra DMA Mode 2 is selected. 0 = Ultra DMA Mode 2 is not selected.
		P	V	9	1 = Ultra DMA Mode 1 is selected. 0 = Ultra DMA Mode 1 is not selected.
		P	V	8	1 = Ultra DMA Mode 0 is selected. 0 = Ultra DMA Mode 0 is not selected.
				7	Reserved
		P	F	6	1 = Ultra DMA Mode 6 and below are supported.
		P	F	5	1 = Ultra DMA Mode 5 and below are supported.
		P	F	4	1 = Ultra DMA Mode 4 and below are supported.
		P	F	3	1 = Ultra DMA Mode 3 and below are supported.
		P	F	2	1 = Ultra DMA Mode 2 and below are supported.
		P	F	1	1 = Ultra DMA Mode 1 and below are supported.
		P	F	0	1 = Ultra DMA Mode 0 is supported.
89				15:8	Reserved
	O	B	F	7:0	Time required for Normal Erase Mode SECURITY ERASE UNIT command.
90				15:8	Reserved
				7:0	Time required for Enhanced Erase Mode SECURITY ERASE UNIT command.
91	O	B	V		Current APM Level Value
92	O	B	V		Master Password Identifier
93	M				Hardware Reset Result The contents of bits (12:0) of this word shall change only during the execution of a hardware reset.
			F	15	Shall be cleared to zero.
			F	14	Shall be set to one.
		P	V	13	1 = Device detected CBLID- above V_{IHB} . 0 = Device detected CBLID- above V_{IL} .

		P	12:8	Device 1 Hardware Reset Result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:
			12	Reserved
		V	11	0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-.
		V	10:9	These bits indicate how Device 1 determined the device number: 00 = Reserved 01 = A jumper was used. 10 = The CSEL signal was used. 11 = Some other method was used or the method is unknown.
			8	Shall be set to one.
		P	7:0	Device 0 Hardware Reset Result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:
			7	Reserved
		F	6	0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected.
		V	5	0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-.
		V	4	0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-.
		V	3	0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics.
		V	2:1	These bits indicate how Device 0 determined the device number: 00 = Reserved 01 = A jumper was used. 10 = The CSEL signal was used. 11 = Some other method was used or the method is unknown.

94	O	B	F	Current AAM value
		B	F	15:8 Vendor's Recommended AAM value.
		B	V	7:0 Current AAM value.
95	O	B	F	Stream Minimum Request Size
96	O	B	V	Streaming Transfer Time – DMA
97	O	B	V	Streaming Access Latency – DMA and PIO
98-99	O	B	F	Streaming Performance Granularity (DWord)
100-103	O	B	V	Total Number of User Addressable Logical Sectors for 48-Bit Commands (Qword)
104	O	B	V	Streaming Transfer Time – PIO
105				Reserved
106	O	B	F	Physical Sector Size/Logical Sector Size
		B	F	15 Shall be cleared to zero.
		B	F	14 Shall be set to one.
		B	F	13 1 = Device has multiple logical sectors per physical sector.
		B	F	12 1 = Device Logical Sector longer than 256 Words.
				11:4 Reserved
		B	F	3:0 2 ^x logical sectors per physical sector.
107	O	B	F	Inter-seek Delay for ISO-7779 Standard Acoustic Testing
108-111	M	B	F	World Wide Name
112-115				Reserved
116				Reserved for TLC
117-118	O	B	F	Logical Sector Size (DWord)
119	M		F	Commands and Feature Sets Supported (Continued from Words 82:84)
			F	15 Shall be cleared to zero.
			F	14 Shall be set to one.
				13:6 Reserved
		B	F	5 1 = The Free-Fall Control Feature Set is supported.

		B	F	4 1 = The DOWNLOAD MICROCODE command with Mode 3 is supported.
		B	F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported.
		B	F	2 1 = The WRITE UNCORRECTABLE EXT command is supported.
		B	F	1 1 = The Write-Read-Verify Feature Set is supported.
				0 Reserved to DDT.
120	M			Commands and Feature Sets Supported or Enabled (Continued from Words 85:87)
			F	15 Shall be cleared to zero.
			F	14 Shall be set to one.
				13:6 Reserved
		B	V	5 1 = The Free-Fall Control Feature Set is enabled.
		B	F	4 1 = The DOWNLOAD MICROCODE command with Mode 3 is supported.
		B	F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported.
		B	F	2 1 = The WRITE UNCORRECTABLE EXT command is supported.
		B	V	1 1 = The Write-Read-Verify Feature Set is supported.
				0 Reserved for DDT.
121-126				Reserved for Expanded Supported and Enabled Settings
127			X	Obsolete
128	O			Security Status
				15:9 Reserved
		B	V	8 Master Password Capability: 0 = High, 1 = Maximum
				7:6 Reserved
		B	F	5 1 = Enhanced Security Erase supported.
		B	V	4 1 = Security Count Expired
		B	V	3 1 = Security Frozen
		B	V	2 1 = Security Locked

		B	V	1 1 = Security Enabled
		B	F	0 1 = Security Supported
129-159			X	Vendor Specific
160	O	N	F	CFA Power Mode
			F	15 Word 160 supported.
			F	14 Reserved
			F	13 CFA Power Mode 1 is required for one or more commands implemented by the device.
			V	12 CFA Power Mode 1 disabled.
			F	11:0 Maximum current in mA.
161-167				Reserved for the CompactFlash Association
168	O	B	F	15:4 Reserved
			F	3:0 Device Nominal Form Factor
169-175				Reserved
176-205	O	B	V	Current Media Serial Number (ATA String)
206	O	B	X	SCT Command Transport
			X	15:12 Vendor Specific
			X	11:6 Reserved
			F	5 The SCT Data Tables command is supported.
			F	4 The SCT Feature Control command is supported.
			F	3 The SCT Error Recovery Control command is supported.
			F	2 The SCT Write Same command is supported.
			F	1 The SCT Read/Write Long command is supported.
			F	0 The SCT Command Transport is supported.
207-208		N		Reserved for CE-ATA.
209	O		F	Alignment of Logical Blocks within a Physical Block
			F	15 Shall be cleared to zero.
			F	14 Shall be set to one.
		B	F	13:0 Logical sector offset within the first physical sector where the first logical sector is placed.

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210-211	O	B	V	Write-Read-Verify Sector Count Mode 3 (DWord)
212-213	O	B	F	Write-Read-Verify Sector Count Mode 2 (DWord)
214	O	B		NV Cache Capabilities
			F	15:12 NV Cache Feature Set version.
			F	11:8 NV Cache Power Mode Feature Set version.
				7:5 Reserved
			V	4 1 = NV Cache Feature Set enabled.
				3:2 Reserved
			V	1 1 = NV Cache Power Mode Feature Set enabled.
			F	0 1 = NV Cache Power Mode Feature Set supported.
215-216	O	B	V	NV Cache Size in Logical Blocks (DWord)
217	M	B	F	Nominal Media Rotation Rate
218				Reserved
219	O	B		NV Cache Options
				15:8 Reserved
			F	7:0 Device Estimated Time to Spin-Up in Seconds.
220	O	B		15:8 Reserved
			V	7:0 Write-Read-Verify Feature Set current mode.
221				Reserved
222	M	B		Transport Major Version Number
				0000h or FFFFh = Device does not report version.
			F	15:12 Transport Type
				0h = Parallel
				1h = Serial
				2h - Fh = Reserved
				Parallel Serial
			F	11:5 Reserved Reserved
			F	4 Reserved SATA Rev 2.6
			F	3 Reserved SATA Rev 2.5
			F	2 Reserved SATA II: Extensions
			F	1 ATA/ATAPI-7 SATA 1.0a
			F	0 ATA8-APT ATA8-AST

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223	M	B	F	Transport Minor Version Number
224-233		N		Reserved for CE-ATA
234	O	B	F	Minimum Number of 512-byte Data Blocks per DOWNLOAD MICROCODE command for Mode 03h
235	O	B	F	Maximum Number of 512-byte Data Blocks per DOWNLOAD MICROCODE command for Mode 03h
236-254				Reserved
255	M	B	V	Integrity Word
		B		15:8 Checksum
		B		7:0 Checksum Validity Indicator

IDENTIFY DEVICE (ECh) OUTPUT

Table 14 lists the output values that are returned when the IDENTIFY DEVICE (ECh) command is issued.



XXXXh = Variable value(s) dependent on the specific controller and flash memory configuration.

Table 14: ECh Command Output

WORD	DATA	DESCRIPTION	NOTES
0	0C5Ah	General Information.	General configuration data.
1	3FFFh	Number of Cylinders	Obsolete. Default number of cylinders: 16383 0x3FFF.
2	C837h	Power-Up Configuration	Configuration for Power-Up in Standby. Device does not require SET FEATURES command to spin-up after power-up and IDENTIFY DEVICE response is complete.
3	0010h	Number of Heads	Obsolete. Default number of heads: 16.
4-5	0000h	Retired	Retired.
6	003Fh	Number of Sectors/Track	Obsolete. Default number of sectors per track: 63.
7-8	0000h	Reserved	Reserved
9	0000h	Retired	Retired
10-19	XXXXh	Serial Number	ASCII String (20 ASCII Characters).
20	0000h	Controller Type	Retired
21	FFFFh	Sector Buffer Size	Retired
22	3000h	Number of ECC Bytes Appended	Obsolete
23-26	XXXXh	Firmware Revision	ASCII String (8 ASCII Characters)
27-46	XXXXh	Model Number	ASCII String (40 ASCII Characters) "STEC VELOCITY SSD".
47	8001h	Read/Write Multiple	Read/Write Multiple support; drive supports the transfer of up to one (1) sector per interrupt on READ/WRITE MULTIPLE commands.
48	0000h	Reserved	Reserved
49	2F00h	Capabilities	Standby Timer defined; IORDY supported; IORDY may not be disabled; DMA supported; LBA supported.

WORD	DATA	DESCRIPTION	NOTES			
50	4000h	Capabilities	Continued from Word 49.			
51-52	0200h	PIO Mode Support	Retired. Slow PIO Mode: 2			
53	0007h	Field Validity	Reserved. Words 54:58, 64:70 and Word 88.			
54	XXXXh	Number of Cylinders	Capacity	Cylinders	Word 54	
			8GB	15,560	40B0h	
			16GB	31,029	7935h	
			32GB	62,037	F255h	
55	0010h	Number of Heads	Capacity	Heads	Word 55	
			8GB	15	000Fh	
			16GB	16	0010h	
			32GB	16	0010h	
56	003Fh	Number of Sectors/Track	Number of Sectors per Track: 63 (003Fh)			
57-58	XXXXh	Current Capacity	Obsolete			
59	0101h	Read/Write Multiple Sector Setting	The current READ/WRITE MULTIPLE command setting: 1 sector per interrupt.			
60-61	XXXXh	Total Addressable Sectors	Total number of user-addressable sectors			
			Capacity	Sectors	Word 61	Word 60
			8GB	15,649,200	00EEh	C9B0h
			16GB	31,277,232	01DDh	40B0h
			32GB	62,533,296	03BAh	2EB0h
62	0000h	Retired	Retired			
63	0007h	Multi-Word DMA Modes	Device supports up to MWDMA Mode 2, set to Mode 0.			
64	0003h	Advanced PIO Transfer Modes	Device supports up to Advanced PIO Mode 3.			
65	0078h	MWDMA Minimum Cycle Time	Minimum MWDMA Cycle Time: 120ns.			
66	0078h	MWDMA Recommended Cycle Time	Recommended MWDMA Cycle Time: 120ns.			
67	0078h	Slow PIO Minimum Cycle Time	Minimum PIO transfer cycle time without flow control: 120ns.			

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WORD	DATA	DESCRIPTION	NOTES
68	0078h	Adv PIO Minimum Cycle Time	Minimum PIO transfer cycle time with IORDY flow control: 120ns.
69	4000h	Command Overlap/Queuing	Reserved
70	0000h	Command Overlap/Queuing	Reserved
71-74	0000h	Reserved	Reserved for PACKET feature set.
75	001Fh	Maximum Queue Depth	Maximum Queue Depth: 32
76	0506h	SATA Capabilities	3.0 Gbps, PHY Event Counter
77	0000h	Reserved	Reserved for SATA.
78	004Ch	Serial ATA Features Supported	SATA features supported; Initial Interface Power Management and Software Settings Preservation.
79	0040h	Serial ATA Features Enabled	SATA features enabled; Software Settings Preservation.
80	01E0h	ATA Major Versions Supported	ATA-8, ATA-7, ATA-6, ATA-5
81	0000h	ATA Minor Versions Supported	Minor version number.
82	346Bh	Command Sets Supported[1]	Supported command sets; SMART, Secure Mode, Power Management, Write Cache, Read Cache, Host Protect Area, Write Buffer, Read Buffer.
83	7D01h	Command Sets Supported [2]	Supported command sets; Download Microcode, SET MAX Security Extensions, 48-Bit Address, Device Configuration Overlay, Flush Cache, Flush Cache Ext.
84	4022h	Command Sets Supported [3]	Supported command/extended feature sets; SMART Self-Test, GP Logging.
85	3469h	Commands/Features Enabled [1]	Supported command/feature sets enabled; SMART, Power Management, Write Cache, Read Cache, Host Protect Area, Write Buffer, Read Buffer.
86	3C01h	Commands/Features Enabled [2]	Supported command/feature sets enabled; Download Microcode, 48-Bit Address, Device Configuration Overlay, Flush Cache, Flush Cache Ext.
87	4022h	Commands/Features Enabled [3]	Default command and feature sets enabled; SMART Self Test, GP Logging.
88	407Fh	UDMA Transfer Mode	Device supports up to UDMA Mode 6, currently set to Mode 6.
89	XXXXh	Secure Erase Completion Time	Time required for completing security erase.

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WORD	DATA	DESCRIPTION	NOTES
90	0000h	Enhanced Security Erase Time	Time required for completing enhanced security erase.
91	0000h	Advanced Power Management	Current Advanced Power Management value.
92	0000h	Master Password Revision Code	Master password revision code.
93	0000h	Hard Reset Result	Result value; 40-conductor cable.
94	0000h	Acoustic Management Value	Recommended acoustic management value: 0x00. Current value: 0x00.
95	0000h	Minimum Stream Request Size	Streaming minimum request size: 0 sectors.
96	0000h	Stream DMA Transfer Time	Streaming transfer time – DMA: 0
97	0000h	Stream Latency	Streaming Access Latency – DMA and PIO.
98	0000h	Streaming Performance Granularity	Granularity: 0µs.
99	0000h	Reserved	Reserved
100-103	XXXXh	48-Bit Maximum LBA	Maximum user LBA for 48-Bit Address feature set.
104	0000h	Streaming PIO Transfer Time	Streaming Transfer Time – PIO: 0µs.
105	0000h	Reserved	Reserved
106	4000h	Physical Sector Size	1 LOG sector = 1 PHY sector.
107	0000h	Inter-Seek Delay	Inter-seek delay for ISO 7779 standard testing.
108-111	XXXXh	World Wide Name	Unique ID: The optional value of the World Wide Name (WWN) for the device.
112-115	0000h	64-Bit World Wide Name (WWN)	Reserved for 64-bit World Wide Name (WWN).
116-126	0000h	Reserved	Reserved
127	0000h	Removable Media Status Notification	Removable Media Status Notification feature set is supported.
128	0001h	Security Status	Security Level = HIGH
129-159	0000h	Vendor	Vendor
160	0000h	CFA Power Requirements	CFAST conforms to Power Level 1
161	0000h	CFAST Specific Support	PHYSLP mode not supported
162-175	0000h	CFA	Key Management Scheme, IDE Mode Timing, PCMCIA Mode Timing, Reserved for CFA.

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WORD	DATA	DESCRIPTION	NOTES
176-195	0000h	Current Media Serial Number	Reserved
196-205	0000h	Current Media Manufacturer	Reserved
206-254	0000h	Reserved	Reserved
255	XXXXh	Checksum	Checksum; Signature.

S.M.A.R.T. SPECIFICATION

OVERVIEW

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology. The S.M.A.R.T. Feature Set protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. S.M.A.R.T. devices attempt to predict the occurrence of near-term degradation or fault conditions. The host system is warned of a negative reliability condition, which subsequently warns the user of the impending risk of data loss. The user can then take appropriate action to minimize the risk.

FEATURE SET SUPPORT

Support for the S.M.A.R.T. Feature Set is indicated by the IDENTIFY DEVICE command response:

Word 82	Bit 0	The S.M.A.R.T. feature set is supported. This information is set during the drive initialization sequence.
Word 84	Bit 1	The S.M.A.R.T. self-test is supported.
Word 84	Bit 0	S.M.A.R.T. error logging is supported.

The enabled indicators for the S.M.A.R.T. feature set are:

Word 85	Bit 0	The S.M.A.R.T. feature set has been enabled via the SMART ENABLE OPERATIONS command. The information is dynamic; the SMART ENABLE OPERATIONS command and SMART DISABLE OPERATIONS command are invoked. The most current setting must be reflected in the output of the IDENTIFY DEVICE command. SMART operations are enabled by default.
Word 87	Bit 1	A "1" indicates that the S.M.A.R.T. self-test is enabled (default).
Word 87	Bit 0	A "0" indicates that the S.M.A.R.T. error logging is enabled (default).

S.M.A.R.T. COMMAND STRUCTURE

COMMAND CODE 0xB0

The command code of 0xB0 will initiate one command of the S.M.A.R.T. command set. The Feature Register is used to select the requested S.M.A.R.T. command.

FEATURE SET

The contents of the Feature Register indicate which subcommand of the S.M.A.R.T. command set is requested.

- Mandatory and Optional status of the subcommand is indicated in the Feature table.
- Use prohibited when the Packet Command feature set is implemented.

PROTOCOL

Non-data, PIO data-in and PIO data-out.

S.M.A.R.T. SUBCOMMANDS

Table 15 lists the commands that are identified by the value placed in the Feature Register.

Table 15: SMART Subcommands

VALUE	COMMAND	NOTES
00h-CFh	Reserved	RSVD
D0h	SMART READ ATTRIBUTE DATA	Optional, supported.
D1h	SMART READ ATTRIBUTE THRESHOLDS	OBS, supported.
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	Mandatory
D3h	SMART SAVE ATTRIBUTE VALUES	OBS, supported.
D4h	SMART EXECUTE OFF-LINE IMMEDIATE	Optional, supported.
D5h	SMART READ LOG	Optional, supported.
D6h	SMART WRITE LOG	Optional, supported.
D7h	Vendor-Specific	OBS
D8h	SMART ENABLE OPERATIONS	Mandatory
D9h	SMART DISABLE OPERATIONS	Mandatory
DAh	SMART RETURN STATUS	Mandatory
DBh	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	OBS, supported
DCh-DFh	Reserved	RSVD
E0h-FFh	Vendor-Specific	VSC

S.M.A.R.T. ATTRIBUTES

Table 16 lists the S.M.A.R.T. attributes that are supported.

Table 16: SMART Attributes

ID	HEX	NAME	DESCRIPTION
1	0x01	Raw Read Error	Count of raw data errors while data is read from the media, including retry errors or data errors (uncorrectable).
2	0x02	Throughput Performance	Average and worst internally measured data transfer rate.
5	0x05	Reallocated Sector Count	Count of reallocated blocks. This is the count of reallocated or remapped sectors during normal operation from the grown defects table.
9	0x09	Power-On Hours	Number of hours elapsed in the Power-On state.
12	0x0C	Power Cycle	Number of Power-Cycle events.
13	0x0D	Soft Read Error Rate	Number of corrected read errors reported to the operating system. SLC: 3 or more bits.
100	0x64	Erase/Program Cycles	Count of Erase/Program cycles for the entire drive.
103	0x67	Translation Table Rebuild	Power backup fault or internal error resulting in loss of system unit tables.
177	0xB1	Wear Leveling Count	Worst case erase count.
178	0xB2	Unexpected Power Loss	This attribute is used to count the number of unexpected power loss events.
180	0xB4	Reserved Block Count	Number of reserved spares for bad block handling.
181	0xB5	Program Fail Count	Count of flash program failures.
182	0xB6	Erase Fail Count	Count of flash erase command failures.
183	0xB7	Runtime Bad Block	Total number of data blocks with detected, uncorrectable errors encountered during normal operation.
184	0xB8	End-to-End Error Detection	Tracks the number of end-to-end internal drive data path errors that were detected.
187	0xBB	Reported Uncorrectable Errors	The number of uncorrectable errors reported at the interface.

ID	HEX	NAME	DESCRIPTION
188	0xBC	Command Timeout	Tracks the number of command time-outs as defined by an active command being interrupted.
194	0xC2	Temperature	Temperature of the base casting.
195	0xC3	Hardware ECC Recovered	Count of ECC errors encountered and corrected using hardware error correction.
196	0xC4	Reallocation Event	Total number of re-mapping events during normal operation and offline surface scanning.
197	0xC5	Current Pending Sector Count	Number of blocks marked suspect due to uncorrectable errors.
198	0xC6	Offline Surface Scan	Number of uncorrected errors that occurred during an offline scan.
199	0xC7	UDMA/SATA CRC Error	Number of CRC errors during UDMA or SATA mode transfers.
200	0xC8	Average Wear Leveling	Average number of block erase counts for all blocks on the solid state drive.
233	0xE9	Number of Write Count	Count of Write commands originating from the host side.

PHYSICAL CHARACTERISTICS

OVERVIEW

This section discusses the materials, weights, storage capacities and physical dimensions relative to the Velocity-4 CFAST Card.

CARD CAPACITIES

Table 17 lists the storage capacity and corresponding LBA (Logical Bit Addressing) and CHS (Cylinder, Head, Sector) information. The CHS Capacity is expressed as User-Addressable LBA Sectors. The extended use of the device shall not reduce the LBA count. The LBA count will remain constant over the life of the card.

Table 17: SSD Capacities

CAPACITY (UNFORMATTED)	LOGICAL BIT ADDRESSING (LBA DATA)	CYLINDER, HEAD, SECTOR (CHS) DATA		
	USER-ADDRESSABLE LBA SECTORS	LOGICAL CYLINDERS	LOGICAL HEADS	LOGICAL SECTORS
8GB	15,649,200	16,560	15	63
16GB	31,277,232	30,029	16	63
32GB	62,533,296	62,037	16	63

MATERIALS

All acceptable materials are HB rated or higher if approved by the safety agencies (UL, CAS, TUV, etc.). All printed circuit boards (PCBs) have a flammability rating of UL94V-0.

CARD WEIGHT

The weight of a card varies according to the specific set of design characteristics. The storage capacity, IC stacking technology (if used), case material, flash controller/memory configuration and form factor all determine the exact weight of a card. Table 18 lists the approximate weights by drive capacity.

Table 18: SSD Weights

CAPACITY	POUNDS	OUNCES	GRAMS
8GB	0.0176	0.282	8
16GB	0.0176	0.282	8
32GB	0.0176	0.282	8

EXTERIOR DIMENSIONS – TYPE I

Figure 7 shows the overall dimensions of CFAST Type I design. The maximum height of the card shall not exceed 3.60mm (0.142 inches).

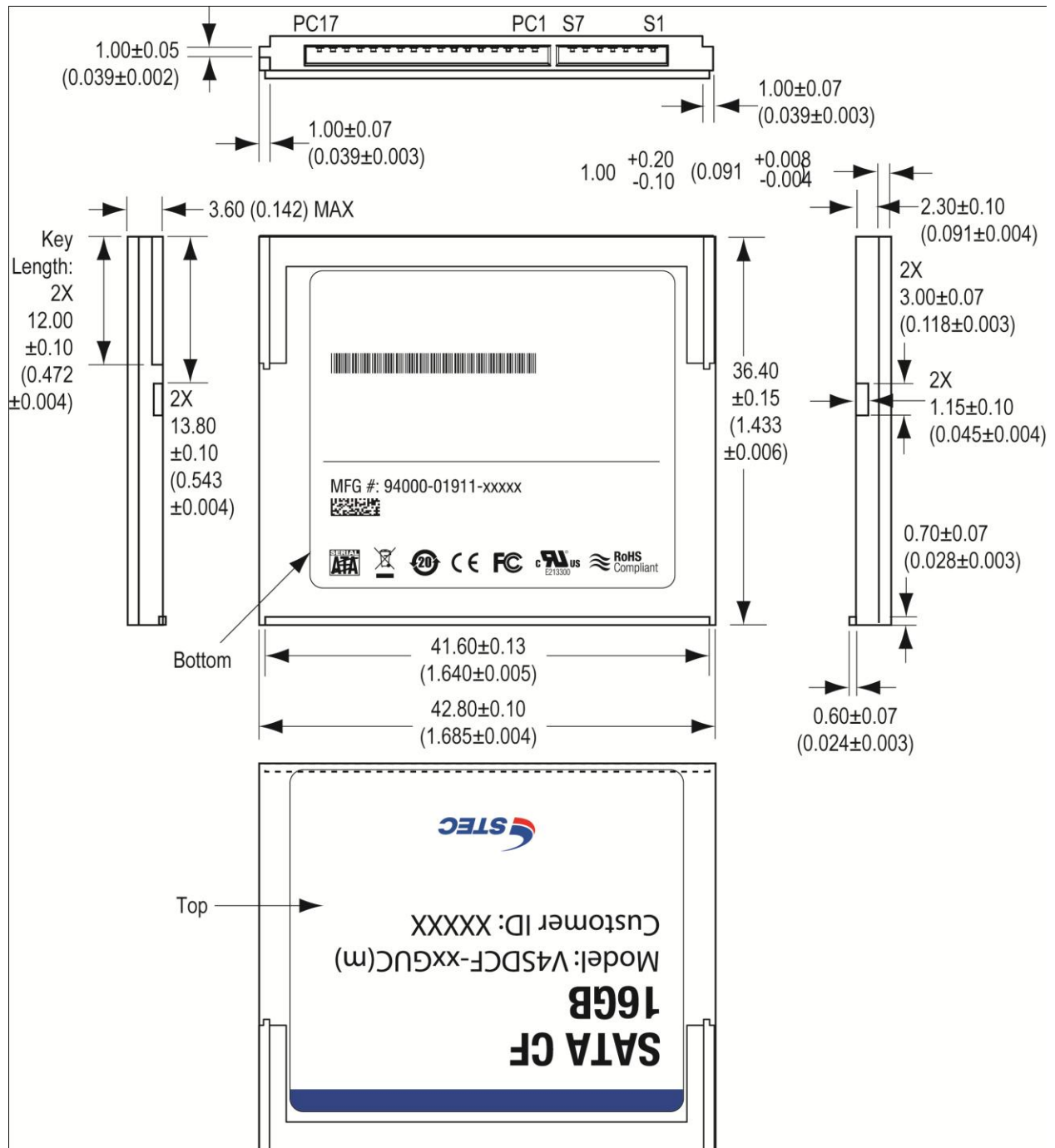


Figure 7: CFAST Type I Dimensions

CONNECTOR LOCATION

Figure 8 illustrates the relative location of the connector.

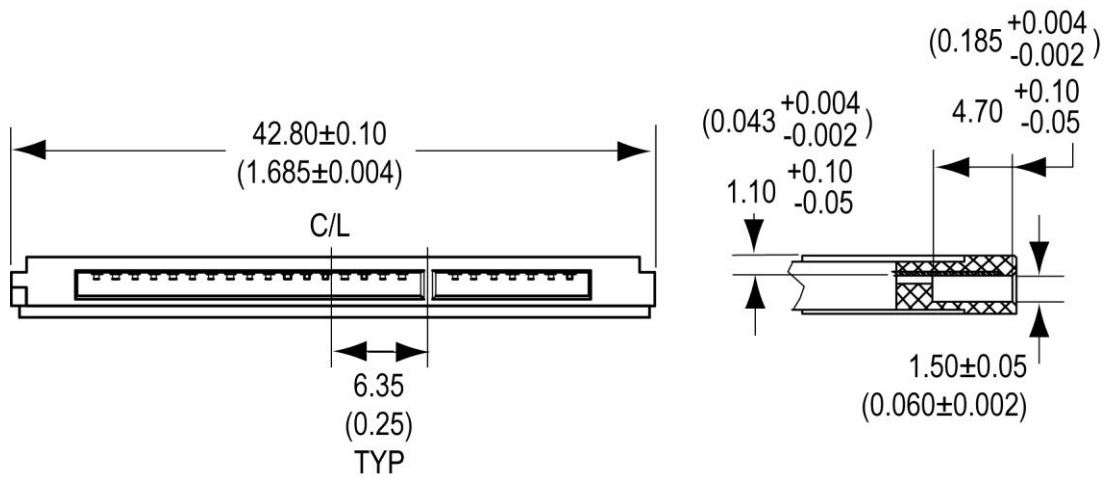


Figure 8: Connector Location

ENVIRONMENTAL CHARACTERISTICS

OVERVIEW

The card is subjected to a series of environmental tests to validate the drive for operation in harsh and mobile conditions. The card will operate to specification within the temperature and relative humidity ranges as outlined in the following sections.

TEMPERATURE

The card operates to specification within the component temperature ranges outlined in Table 19. Non-operating temperatures apply to shipping and storage requirements.

Table 19: Temperatures

TEMPERATURE	CELSIUS (°C)		FAHRENHEIT (°F)	
	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
Commercial	0	70	32	158
Industrial	N/A	N/A	N/A	N/A
Non-Operating	-25	70	-13	158

RELATIVE HUMIDITY

Table 20 lists the operating and non-operating (storage/shipping) relative humidity criteria.

Table 20: Relative Humidity Criteria

OPERATING	VALUE
Relative Humidity Range (Non-Condensing)	5% to 90%
Maximum Wet Bulb Temperature	20°C
Maximum Temperature Gradient	20°C/Hour
NON-OPERATING	VALUE
Relative Humidity Range (Non-Condensing)	5% to 95%
Maximum Wet Bulb Temperature	35°C
Maximum Temperature Gradient	30°C/Hour

SHOCK AND VIBRATION

This section specifies the capacity of the card to withstand shock and vibration.

RESONANCE

Resonance may occur if the card is placed in an enclosure. It is the responsibility of the user to design the mounting such that the card movement is within the specified ranges despite resonance.

FAILURE CRITERIA

Test failures are defined as:

- Any single hard error (unrecoverable error)
- Damage that renders the product inoperable
- Failure to meet performance specifications

SHOCK

The card is shock-tested in accordance with JESD22-B110 and will perform without any errors or any transfer rate degradation after being tested under the conditions outlined in Table 21.

Table 21: Shock Test Conditions

ACCELERATION	DURATION	WAVEFORM	TOTAL SHOCKS	NOTES
350G Peak	0.6ms	Half-Sine	30	Along the $\pm X$, $\pm Y$ and $\pm Z$; axis.

VIBRATION

For sinusoidal vibration, the card is tested in accordance with JESD22-B103 and will perform without any errors or any transfer rate degradation after being tested under the conditions outlined in Table 22.

Table 22: Vibration Conditions

ACCELERATION	DURATION	WAVEFORM	FREQUENCY RANGE	NOTES
20G Peak	60min/axis	Sine	20Hz – 2000Hz	Along the X, Y and Z axis.

DROP TEST

The card will withstand three (3) drops on a concrete floor from 1.524m (60 inches) on each of the six (6) axes, $\pm X$, $\pm Y$ and $\pm Z$, without any damage when packaged.

SYSTEM REQUIREMENTS



There is a risk of electrocution! Use extreme caution when handling the solid state drive and while connecting it to a power source. Observe all applicable electrical safety rules while installing the solid state drive. Make sure to read and thoroughly understand this section before attempting to install the drive.

SATA COMPATIBILITY

The card can be used in any environment that has a CFAST Card slot and SATA 1.0 or greater operating system support. The card is compliant to CFAST 1.0 and SATA 2 standards. If the system fails to recognize the card, make sure the most recent drivers for the CFAST Card slot are installed. If the CFAST Card slot is connected to the motherboard, the drivers are provided by the motherboard manufacturer. If the CFAST Card slot is connected to a PCI card, contact the PCI card manufacturer. Alteration of the operating system is not required; the card will support all ATA and ATAPI devices, including CDs, DVDs, tape devices, high-capacity removable devices, Zip drives, and CDRWs.

CONFIGURATION

Serial ATA devices do not support Primary/Secondary device negotiation. The card operates as a single configuration mode (Primary/Device 0) device. Each CFAST card requires a separate slot that connects directly to a SATA host adapter, a SATA port on the motherboard, or a backplane connector. Since most motherboards with Serial ATA connectors do not allow BIOS adjustments, changes are not typically required to add a SATA device. However, if replacing the boot drive, it may be necessary to change the boot order in the BIOS so that the computer boots from the Serial ATA controller.



CFAST Cards are SATA devices and can be used in the same system with PATA drives provided that both interfaces are supported on the motherboard or with a host adapter. The user can add SATA compatibility to an existing system without having to remove any existing PATA drives.

DRIVE ORIENTATION

The card can be installed in any number of orientations within the host. The card will operate and meet all the requirements as outlined in this specification regardless of the card slot orientation and when tilted $\pm 15^\circ$ from any of these positions. See Figure 9.

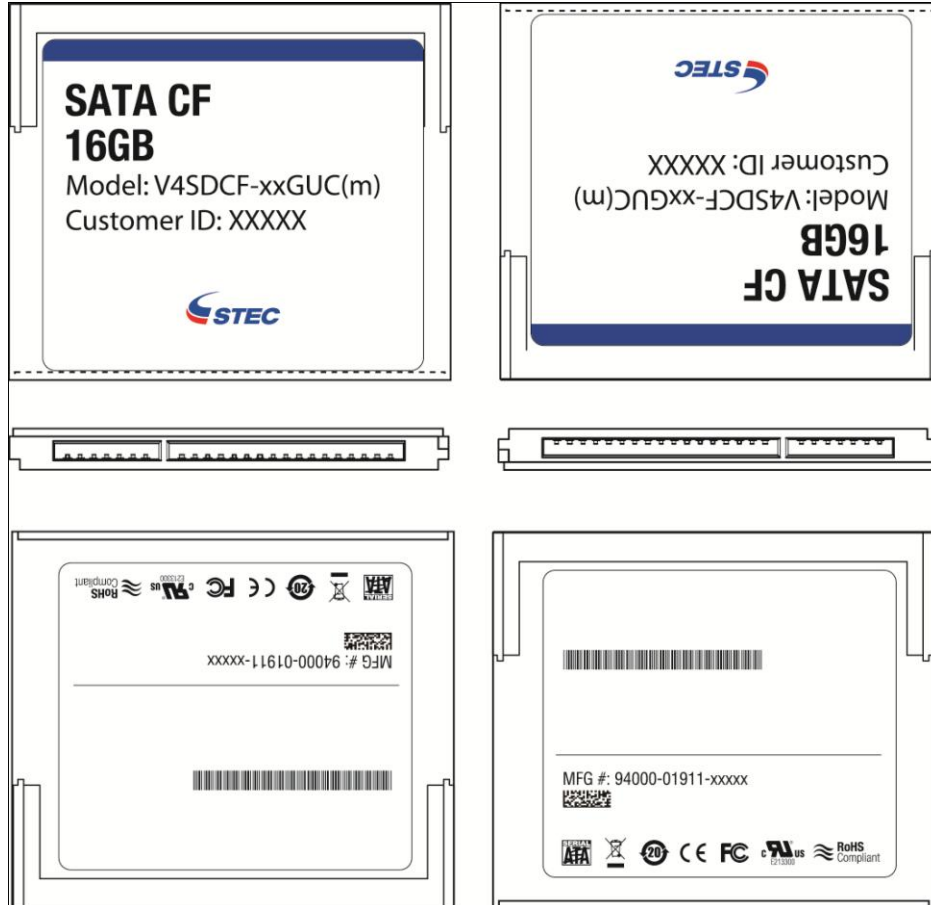


Figure 9: Possible Card Orientations

PRIMARY HEAT GENERATION AREA

Figure 10 indicates the approximate location of the primary heat generation area. See [Cooling Requirements](#).



Exercise caution when handling the drive after extended operation. The heat generated by the internal circuitry can be substantial.

Primary Heat Generation Area

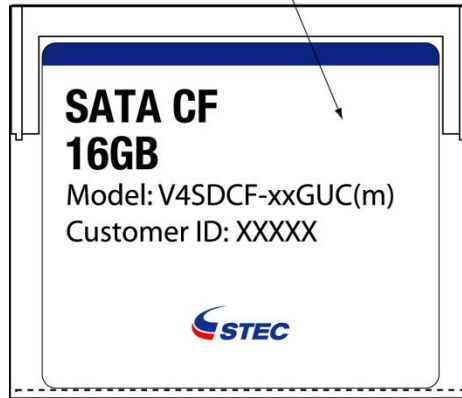


Figure 10: Primary Heat Generation Area

COOLING REQUIREMENTS

The host enclosure may remove heat by conduction, convection, or other forced airflow to maintain the required operating temperature range. The air can flow in the direction as indicated in Figure 11, or in the opposite direction, front-to-back, back-to-front, or side-to-side.

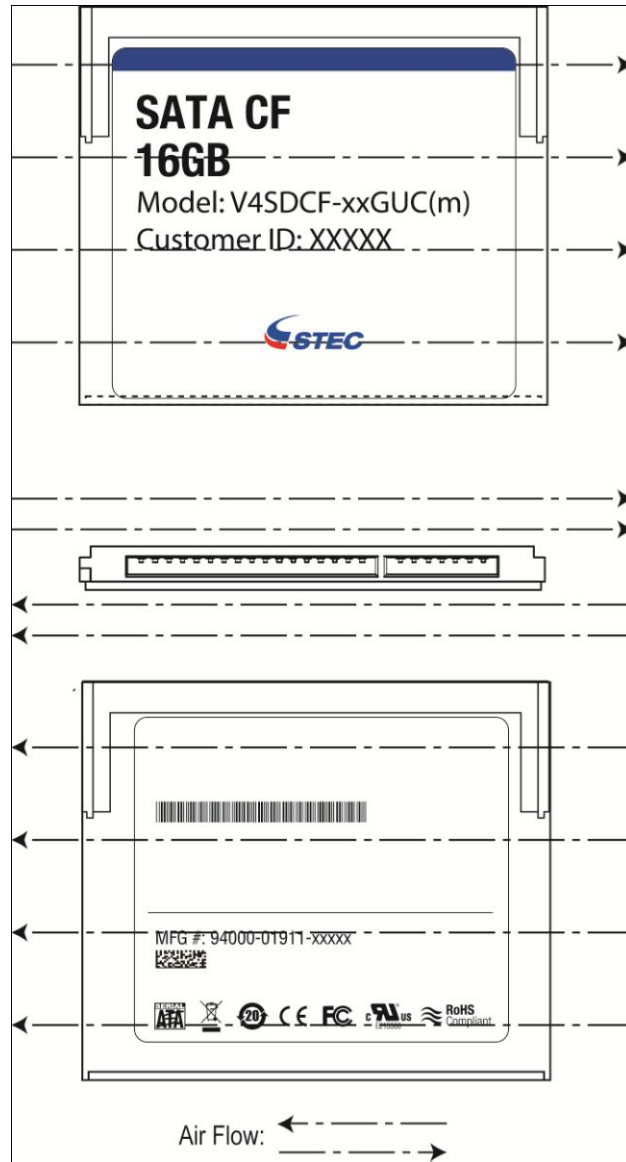


Figure 11: Suggested Air Flow Patterns for Cooling

OPERATING SYSTEM SPECIFICATIONS

The card is compatible with Microsoft Windows® and alternative operating systems. The card is low-level formatted at the factory (00h in all data sectors). However, the card must be partitioned and high-level formatted. The card can be formatted as a boot or data storage drive using any standard disk partitioning and formatting utility.

MICROSOFT OS COMPATIBILITY

The card is fully compatible with the following Microsoft operating systems, using the native drivers supplied with the OS:

- Windows 2000, Service Packs 2, 3 and 4
- Windows 2000 Server, Advanced Server
- Windows XP Home and Windows XP Professional, Service Packs 1 and 2
- Windows XP, 64-Bit Extended
- Windows XP, Embedded
- Windows 2003 Standard, Enterprise, 64-Bit, Web, Datacenter, Small Business Server
- Windows Vista
- MS-DOS
- Windows Pre-boot Environment (WinPE)

The card is compatible with the current versions of the MS-DOS real-mode drivers bundled with any of the Microsoft operating systems for reading files from optical media.

ALTERNATIVE OPERATING SYSTEMS

The card is fully compatible with the following operating systems, using the native drivers supplied with the OS:

- Red Hat Linux
- SUS Linux
- VXWorks
- VMWare/Hypervisor
- CISCO IOS/ROMON
- FreeBSD

SYSTEM POST, BOOT AND RESUME TIMES

The effect on the time required for the system to POST, boot and resume under Microsoft Windows XP is minimized. Device implementation will target minimum impact to such. The drive also complies with the Microsoft Fast Boot/Fast Resume Requirement, which is ≤ 2.5 seconds for Resume from Standby (S3), and ≤ 20 seconds for Resume from Hibernate (S4).

DIAGNOSTIC SOFTWARE

The computer or system manufacturer is responsible for providing any diagnostic software or utilities.

REGULATORY COMPLIANCE

MARKING, APPROVALS AND SUPPORTING DOCUMENTATION

The card may have the following marks, approvals and documentation as outlined in Table 23.

Table 23: Regulatory Marks and Documentation

MARK/APPROVAL	DOCUMENTATION	MARK
BSMI (Taiwan)	Certificate with Applicant Code Number	No
Canada	CAN/CSA C22.2 60950-1:2003	Yes
CE	EN 60950-1/A11:2004	Yes
C-TICK (Australia)	Declaration of Conformity (DoC), with supplier code number and a Letter of Authorization from the supplier giving the OEM permission to import and sell the product using the STEC Inc. C-TICK.	No
EIP (China RoHS)	Electronic Information Products (EIP) label.	Yes
EU (EC)	European Union. Low Voltage Directive 73/23/ECC for Product Safety and EMC Directive 89/336/ECC EN55022, 1998. EN55024 for Emissions and Immunity, 1998. All applicable amendments. Equipment may demonstrate compliance with the directive by being approved to a recognized standard by an EC (EU) recognized agency, such as TUV or VDE and a signed Declaration of Conformity, and the CE Mark on the device.	Yes
FCC (USA)	Federal Communications Commission Declaration of Conformity	Yes
KCC (Korea)	Korean Communications Commission (KCC). The KCC mark is required to be placed on approved electronic and electrical devices starting November 1, 2008.	No
TUV/SEMKO/UL/etc.	Germany, being a member of the EC (EU), is bound by the Low Voltage Directive and EMC Directive. The Equipment Safety Law of Germany requires that equipment will be "...in accordance with the generally recognized with the generally recognized rules of technology and the work safety and accident prevention regulations..." Equipment may demonstrate compliance with the directive by being approved to a recognized standard by an EC (EU) recognized agency such as TUV or VDE. STEC Inc. will provide a CB Certificate and Test Report with the supporting Type Certificate (e.g., TUV Certificate, from the Agency that approved the CB Test Report).	No
USA	UL 60950-1/R: 2007-10	Yes
VCCI (Japan)	Certificate or Declaration of Conformity. A self-declaration that the product has been evaluated in a VCCI-compliant laboratory is sufficient.	Yes

RESTRICTION OF HAZARDOUS MATERIALS (ROHS DIRECTIVE)



The cards comply with the European Union (EU) Restriction of Hazardous Substances (RoHS) Directive, EU 2002/95/EC. The SSDs meet the requirements for the following banned substances: Lead, Mercury, Hexavalent Chromium, Cadmium, Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ether (PBDE). 2008-10-22.

FCC DECLARATION OF CONFORMITY

The Federal Communications Commission (FCC) Declaration of Conformity (DoC) will contain the following:

- Product type and model number
- Marks and countries (e.g. CE, FCC, C-TICK)
- The appropriate technical statement(s) required by the respective regulatory agencies
- STEC name and address
- STEC signature
- List of all applicable standards to which the drive conforms

FCC CLASS A WARNING



The card carries the FCC mark in accordance with related Federal Communications Commission (FCC)–USA directives. This device complies with Part 15 of the FCC Rules.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Section 15 of the FCC Rules. Class A certification is for business or commercial use. These limits are designed to provide reasonable protection against harmful interference in a commercial or business installation. This equipment can generate, use and radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. The operation of this equipment in a residential area is likely to cause harmful interference. It is the responsibility of the user to correct the interference at his or her expense.

Modifications made to this device without authorization from STEC INC may result in the device violating the FCC requirements for Class A digital devices. In that event, the right of the user to use the equipment may be limited by FCC regulations, and the user may be required at his or her expense to correct any interference to radio or television communications.

CB CERTIFICATE AND CB REPORT

STEC Inc. will provide a complete CB Report. These documents will include the current and voltage ratings, and prove compliance with the currently applicable versions of IEC 60950-1:2001, Safety of Information Technology Equipment, including all national deviations.

STEC Inc. will also provide the EMC test report indicating compliance with the currently applicable versions of:

- EN-55022:1998 (Emissions)
- EN-55024:1998 (Immunity)
- FCC 47CFR Part 15 Class B

FLAMMABILITY RATINGS

The PCBs, foam and plastic materials all have a UL recognized from class of V-1, HF-1 or VTM-1 or better. Smaller mechanical parts (cable ties, washers, screws, PC board mounts, etc.) that would not significantly contribute to a fire are made of materials with a UL recognized frame class of V-2.

RADIO FREQUENCY EMISSIONS

The card has passed radiated emissions testing (10 meter chamber) with a minimum margin of 4dB below the EN55022 radiated emissions limits in all applicable customer platforms, without any required changes to the system platforms.

Emissions testing in a 3 meter chamber for over 1GHz per the FCC limit for Class B was performed up to 2GHz with the -4dB margin relative to the FCC Class B limit.

In preparation for the new CISPR 22 standard change that may go into effect in the year 2007, the card will pass EMI tests up to the higher frequency of either 6GHz or the fifth harmonic of the highest signal on the drive. This requirement is applicable to all products being qualified after this version is released. The specification limits are listed in the following table.

Table 24: EMI Specification Limits

CLASS	DESCRIPTION
Class B	1 to 3 GHz is 50dB (uV/m) @ 3 m
Class B	3 to 6 GHz is 54dB (uV/M) @ 3 m

RADIO FREQUENCY IMMUNITY REQUIREMENTS

This specification is targeted as part of the design for quality and reliability expectations and is not part of the regulatory requirements. The card's meet the following radio frequency immunity requirements:

- 3 V/m over frequency range of 80 MHz to 1 GHz
- The signal will be amplitude modulated with a 1KHz sine wave to a depth of 80%
- Failure Criteria: More than 10% throughput degradation

EMI TESTING

STEC conducts EMI testing at STEC approved test facilities, but recommends that customers also conduct EMI testing at their own approved EMI test facilities to ensure correlation with EMI testing of their end systems.

VERIFICATION SAMPLES

STEC will submit three worst-case drives used to obtain the emissions test data previously obtained from the customer's test facilities for verification testing. The Regulator Engineer will use these drive samples, and others among those submitted for qualification, for emissions verification in the customer's systems.

VERIFICATION TESTING

Verification testing will be performed by the customer's Compliance Peripheral Group.

ORDERING INFORMATION

PART NUMBER DECODER

Example: A V4SDCF-32UCM-XXX would be a Velocity-4 CFAST Card with a data rate of 3.0 Gb/second and a capacity of 32 gigabytes; the card would be RoHS Complaint have components rated for the commercial temperature range. The memory subsystem would consist of Multi-Level Cell (MLC) NAND EEPROM flash devices.

1	2	3	4	5	6	-	7	8	9	10	-	11
V4	(I)	S	D	CF	(B)	-	xx	U	(T)	(M)	-	XXX

KEY

1	PRODUCT FAMILY	
	V4	Velocity-4
2	IOPS OR STANDARD	
	I	IOPS SSD (Not Applicable)
	BLANK	Standard SSD
3	INTERFACE	
	S	SATA 2.6
4	INTERFACE BANDWIDTH	
	D	3.0 Gb/SECOND
5	FORM FACTOR	
	CF	CFAST Type I.
6	GENERATION	
	BLANK	1 st Generation (GEN 1)
7	CAPACITY	
	xx	16 or 32 Gigabytes
8	COMPLIANCE	
	U	RoHS Compliant (Pb-free)
9	TEMPERATURE RATING	
	C	0°C – 70°C (Commercial)
	I	N/A
10	NAND FLASH DEVICES	
	M	MLC (Multi-Level Cell) NAND
	T	SLC (Single-Level Cell) NAND
11	CUSTOMER SPECIFIC	
	XXX	Internal use only.

VELOCITY-4 SATA CFAST 7+17 PIN SSD PRODUCT MANUAL

PART NO: V4SDCF-xxU(T)(M)-XXX
 REVISION NO: 1.8

MANUAL NO: 61000-06652-108
 REVISION DATE: 10/10/2011

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WARRANTY

LIMITED WARRANTY

STEC Inc. ("STEC") Solid State Drives ("SSD") are warranted against defects in material and workmanship, and will operate in substantial conformance with their respective specifications under normal use and service for:

- A period of two (2) years for SLC-based (Single-Level Cell NAND devices) from the date of shipment.
- A period of one (1) year for MLC-based (Multi-Level Cell NAND devices) from the date of shipment.

Subject to the conditions and limitations set forth below, STEC will, at its own option, either repair or replace any defective SSD product that proves to be defective by reasons of improper workmanship or materials, if buyer notifies STEC of such failure within the stated warranty period. Products repaired or replaced during the applicable warranty period shall be covered by the foregoing warranties for the remainder of the original warranty period or ninety (90) days from the date of reshipment, whichever is longer. Parts used to repair products or replacement products may be provided by STEC on an exchange basis, and will be either new or refurbished to be functionally equivalent to new.

STEC DISCLAIMS ALL OTHER WARRANTIES, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, WITH RESPECT TO ITS PRODUCTS AND ANY ACCOMPANYING WRITTEN MATERIALS. FURTHER, STEC DOES NOT WARRANT THAT SOFTWARE WILL BE FREE FROM DEFECTS OR THAT ITS USE WILL BE UNINTERRUPTED OR REGARDING THE USE, OR THE RESULTS OF THE USE OF THE SOFTWARE IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY OR OTHERWISE.

STEC is not responsible for updates or functionality of third-party software. Software is provided with notices and/or licenses from third parties that govern your use.

MODIFICATIONS

Any modifications made to this device that are not expressly approved by STEC will void the user's warranty. All wiring external to the product should follow the provisions of the current edition of the National Electrical Code.



61000-06652-108

Release 1.8

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