

4GB to 32GB
mPCI-Express IDE Card
Preliminary



SLMPCI_xGM4U-M

Solid-State Memory Card
(No Moving Parts)

Capacity: 4GB - 32GB

ATA-7 Compatible

ATA Transfer modes:

UDMA 0-6, MWDMA 0-2, PIO 0-4

Supports TrueIDE

Form Factors:

- mPCI-Express

Advanced Wear-Leveling for
Greater Flash Endurance

3.3V Power Supply

Commercial Operating Temperature
Ranges

Full Data-Path Protection with
built-in ECC Engine

10 Year Data Retention

RoHS-6 Compliant

General Description

The PCI Express Mini Card format has become the format of choice for the emerging ultra-mobile PC category. With its small footprint and industry-standard design, the mPCIe format is an ideal fit for embedded solid state storage because it allows for high capacities and high performance while ensuring compatibility in ultra-mobile applications.

Leveraging STEC's proprietary, high performance MACH4 SSD controller, the Express Mini Card offers extremely high-performance (up to 90MB/s) and high capacities up to 32GB. The result is a no-compromise solid state storage solution providing ultra-mobile system designers with a true plug-n-play storage device, allowing for short design cycles and fast time to market.

Flash memory has quickly become the product of choice for applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature, especially important to mobile applications. Because the MACH4 PCI Express Mini Card uses NAND flash technology (e.g. no moving parts), it is more reliable and has much lower latency compared to a traditional hard disk drive, while consuming half the power (approximately 1 watt compared to 2 watts for a typical mobile hard disk drive). STEC's MACH4 PCI Express Mini Card also adheres to the PCI-SIG Express Mini Card mechanical specification as well as industry compliance and regulatory standards including UL, FCC, RoHS, and ATA-7. This combined with a proprietary state-of-the-art flash memory controller supporting key flash management features including advanced wear-leveling and error checking and correction as well as drive monitoring (SMART), provides OEMs with the flexibility to address customer-specific applications with the industry's highest reliability and endurance. Key features include:

- Full datapath protection with built-in 8-bit BCH ECC engine to detect and correct up to 8-bit errors per 512 Bytes of data
- Sophisticated bad block management and wear leveling algorithms dramatically enhance flash memory endurance
- Power-down data protection ensures data integrity in case of power loss
- Lifecycle management feature allows users to monitor the card's lifetime by monitoring the card's remaining spare blocks

STEC's MACH4 mPCI-Express IDE Card offers the highest reliability and tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with temperature testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments. In addition to custom hardware and firmware designs, STEC also offers value-added services including:

- Custom labeling and packaging
- Custom software imaging and ID strings
- Full BOM control and product change notification
- Total supply-chain management to ensure continuity of supply
- In-field application engineering to help customers through product design-ins

** Actual throughput may vary depending on hosts system and configuration; all performance numbers are based on card being configured in TrueIDE mode with UDMA-6 supported.*

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1.0 Ordering Information

Table 1 lists the ordering part number for custom STEC MACH4 mPCI-Express IDE Card.

Table 1: Ordering Information

Part Number	Form Factor	Capacity
SLMPCI4GM4U-M	mPCI-Express	4 GBytes
SLMPCI8GM4U-M	mPCI-Express	8 GBytes
SLMPCI16GM4U-M	mPCI-Express	16 GBytes
SLMPCI32GM4U-M	mPCI-Express	32 GBytes

Legend:

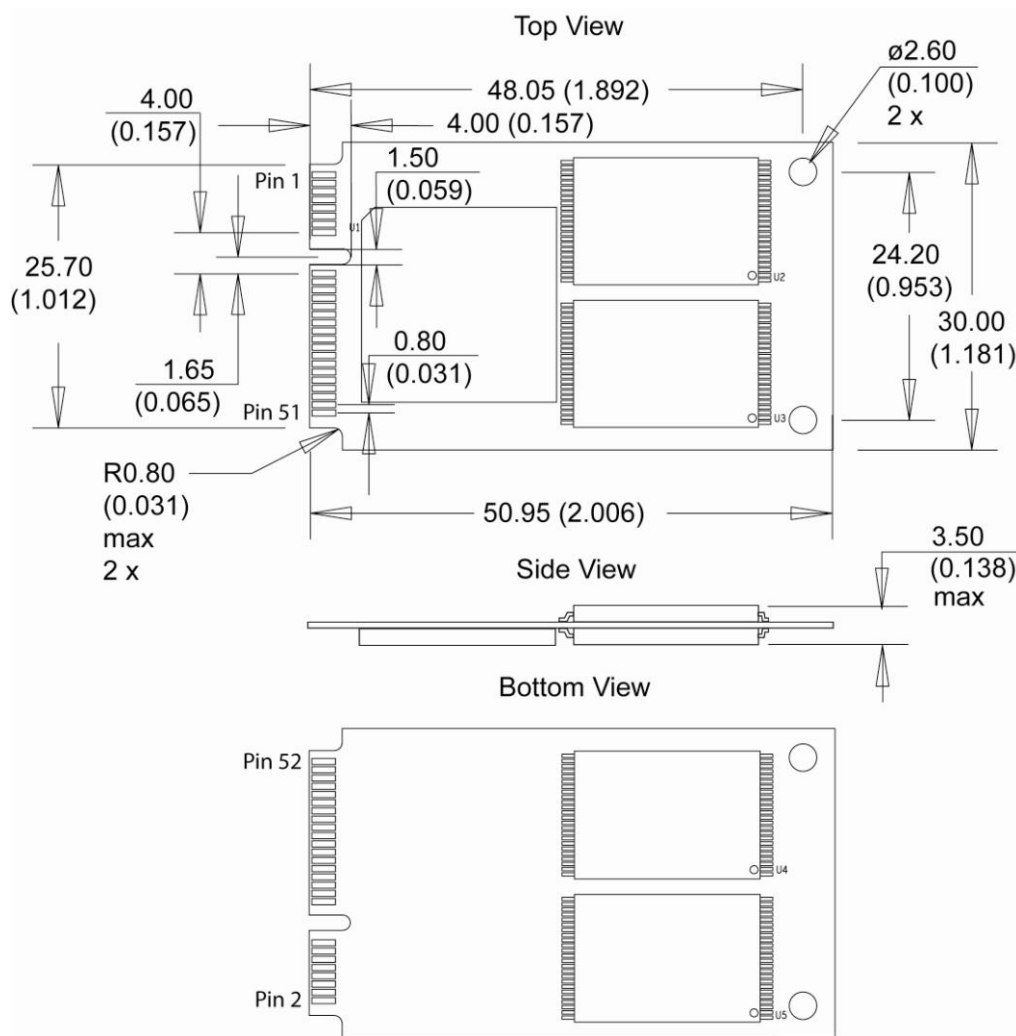
- **SLMPCI** = STEC custom mPCI-Express IDE Card part number prefix.
- **G** = proceeding capacity is in Gigabytes.
- **M4** = MACH4 controller
- **U** = RoHS-6 compliant lead-free.
- **Part numbers without (I)** = Commercial temperature range (0°C to 70°C).
- **M** = MLC flash components

1.1 Package Dimensions and Pin Locations

Table 2 and Figure 1 show the mechanical dimensions of the mPCI-Express IDE Card.

Table 2: Mechanical dimensions mPCI-Express IDE Card

Parameter	Value
Length	25.70 ± 0.10 mm (1.012 ± 0.004 in)
Width	50.95 ± 0.10 mm (2.006 ± 0.004 in)
Height	3.50 (0.138) max



- Notes:
1. All dimensions are in mm (inches).
 2. Tolerances are ± 0.100 (0.004).

Figure 1: Mechanical dimensions mPCI-Express IDE Card

1.2 Pin Assignments

Table 3: mPCI-Express IDE Card Pin Assignment

Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
1	D00	I/O	27	GND	Ground
2	D15	I/O	28	-IORD HSTROBE -HDMARDY	I
3	D01	I/O	29	GND	Ground
4	GND	Ground	30	-DMACK	I
5	D02	I/O	31	NC	-
6	D14	I/O	32	DMARQ	O
7	D03	I/O	33	NC	-
8	D13	I/O	34	GND	Ground
9	GND	Ground	35	GND	Ground
10	D12	I/O	36	NC	-
11	D04	I/O	37	A00	I
12	D11	I/O	38	NC	-
13	D05	I/O	39	A01	I
14	D10	I/O	40	GND	Ground
15	GND	Ground	41	A02	I
16	D09	I/O	42	IORDY -DDMARDY DSTROBE	O
17	D06	I/O	43	NC	-
18	GND	Ground	44	INTRQ	O
19	D07	I/O	45	NC	-
20	D08	I/O	46	-CS0	I
21	GND	Ground	47	VCC	Power
22	-RESET	I	48	-CS1	I
23	NC	-	49	VCC	Power
24	-IOWR STOP	I	50	GND	Ground
25	NC	-	51	VCC	Power
26	GND	Ground	52	-DASP	I/O

Legend: "-" = Low active

1.3 Signal Description

Table 4: mPCI-Express IDE Card Signal Description

Signal Name	Type	Pin Number	Description
-DASP (True IDE Mode)	I/O	52	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15-D00 (True IDE Mode)	I/O	2, 6, 10, 12, 14, 16, 20, 19, 17, 13, 11, 7, 5, 3, 1,	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (True IDE Mode except UDMA protocol active) STOP (All Modes: UDMA protocol active)	I	24	In True IDE Mode, this signal has the same function as in PC Card I/O Mode. In all modes, while UDMA mode protocol is active, the assertion of this signal causes the termination of the UDMA data burst.
-IORD (True IDE Mode except UDMA protocol active) -HDMARDY (All Modes: UDMA protocol DMA Read) HSTROBE (All Modes: UDMA protocol DMA Write)	I	28	In True IDE Mode, this signal has the same function as in PC Card I/O Mode. In all modes when UDMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive UDMA data-in bursts. The host may negate -HDMARDY to pause an UDMA transfer In all modes when UDMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an UDMA data-out burst
INTRQ (True IDE Mode)	O	44	In True IDE Mode, this signal is the active high interrupt request to the host.
A2-A0 (True IDE Mode)	I	41, 39, 37	In True IDE Mode only, A2:A0 are used to select the one of eight registers in the Task File. The remaining address lines should be grounded.
-CS0, -CS1 (True IDE Mode)	I	46, 48	In the True IDE Mode, -CS0 is the chip enable for the task file registers while -CS1 is used to select the Alternate Status Register and the mPCI-Express IDE Card Control Register.
-DMACK (True IDE Mode)	I	44	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the DMARQ signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.
DMARQ (True IDE Mode)	O	32	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating -DMARQ, and re-asserting -DMARQ if there is more data to transfer. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 and -CS1 shall be held

Signal Name	Type	Pin Number	Description
			negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation.
IORDY (True IDE Mode except UDMA protocol active) -DDMARDY (All Modes: UDMA Write protocol active) DSTROBE (All Modes: UDMA Read protocol active)	O	42	This signal is not used by the mPCI-Express IDE Card, and is pulled up to VCC through a 4.7K ohm resistor. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burs.
GND (True IDE Mode)	-	4, 9, 15, 18, 26, 27, 29, 34, 35, 40, 50	Ground
VCC (True IDE Mode)	-	47, 49, 51	+ 3.3V power
-RESET (True IDE Mode)	I	22	In the True IDE Mode this input pin is the active low hardware reset from the host.

1.4 Performance

Table 5: mPCI-Express IDE Card Read/Write Performance

Parameter	Value
Data transfer rate to/from host	133 MBytes/s (burst)
Sustained read	up to 85 MBytes/s
Sustained write	up to 25 MBytes/s

Note: Performance may vary under extreme temperatures.

1.5 CHS Parameters

Table 6: CHS Parameters per capacity

Capacity	Logical Block Addresses (LBA)	Cylinders (C) (standard)	Heads (H)	Sectors/Track (S)
4GB	7,502,544	7,443	16	63
8GB	15,005,088	14,886	16	63
16GB	30,093,840	29,855	16	63
32GB	60,187,680	59,710	16	63

Note: The unformatted capacity of the card may be less than the perceived or stated capacity on the label. Please use the LBA count in this table for reference.

1.6 Standards Compliance

STEC products specified in this document are certified for compliance with the following industry standards:

- ATA-7
- UL 950
- CE, and FCC Class B & D
- RoHS

1.6.1 CE and FCC Class B & D

The STEC products specified in this document meet the following requirements and limits of the European Standards:

- Class B requirements of the following European Standard:
EN 55022: 1998 – “Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement”
- Class D limits of the following European Standards:
EN 61000-3-2 “Electromagnetic compatibility (EMC) Part 3-2: Limits – Limits for harmonic current emissions (equipment input current up to and including 16 A per phase)”
EN 61000-3-3: 1995 – “Part 3: Limits – Section 3: Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with rated current ≤ 16A”
EN 55024 – “Information technology equipment – Immunity characteristics – Limits and methods of measurement”

1.6.2 RoHS

STEC certifies that its products do not contain any of the restricted substances as stated below and are in compliance with RoHS EU directive 2002/95/EC, specifically:

- Mercury (Hg)
- Cadmium Cd)
- Chromium VI (Cr +6)
- Polybrominated biphenyl (PBB)
- Polybrominated biphenyl ether (PBDE)
- Lead (Pb)

Materials used in the STEC’s products are limited to the following:

- Steel, Nylon 6/6, PCB laminate
- Copper, Gold, Nickel
- Silicon on ICs and Components
- Polyester on Labels

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Table 7: mPCI-Express IDE Card Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Commercial Operating Temperature	Ta1	0	25	70	°C
VCC voltage (3.3V)	VCC3.3	2.97	3.3	3.63	V

2.2 Reliability

Table 8: mPCI-Express IDE Card Endurance & Data Reliability

Parameter	Value
Data reliability	Bit Error rate 10E-14 (NAND flash)
Data retention	10 years

2.3 Shock, Vibration, and Humidity

Table 9: mPCI-Express IDE Card Shock, Vibration & Humidity

Parameter	Value
Shock	1.5K G peak, 0.5ms pulse duration, five (5) pulses per each of six (6) directions (per JEDEC JESD22 standard, method B110)
Vibration	20 G peak, 20Hz-2000Hz, 4 cycles per direction (per JEDEC JESD22 standard, method B103)
Humidity	85°C 85% RH, 500 hrs

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 10: mPCI-Express IDE Card Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage	Vin, Vout	-0.5 to VCC +0.5	V
Storage temperature range	Tstg	-65 to +150	°C

3.2 DC Characteristics

Measurements at Recommended Operating Conditions unless otherwise specified.

Table 11: mPCI-Express IDE Card DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VIL (3.3V)	Input LOW Voltage	-0.3	-	+0.6	V	VCC= 3.3V
VIH (3.3V)	Input HIGH Voltage	2.4	-	VCC +0.3	V	VCC= 3.3V
VOL	Output LOW Voltage		-	0.8		VCC= 3.3V
VOH	Output HIGH Voltage	VCC-0.8	-	-	V	VCC= 3.3V
ICC(SB)	Standby Current	-	24	-	mA	ICC at VCC= 3.3V
ICC(Idle)	Idle Current	-	90	-	mA	ICC at VCC= 3.3V
ICC	Operating Current	-	120	-	mA	ICC at VCC= 3.3V
RPU	Pull-Up Resistance	100	-	-	K ohms	
RPD	Pull-Down Resistance	100	-	-	K ohms	

3.3 AC Characteristics

Measurements at Recommended Operating Conditions, unless otherwise specified.

3.3.1 True IDE Mode Register Access

Table 12: True IDE Mode Register Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time (min)	t0	600	383	330	180	120	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	ns
-IOWR data setup (min)	t3	60	45	30	30	20	ns
-IOWR data hold (min)	t4	30	20	15	10	10	ns
-IORD data setup (min)	t5	50	35	20	20	20	ns
-IORD data hold (min)	t6	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	ns
Address valid to -IOCS16 release (max)	t8	60	45	30	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	ns

3.3.2 True IDE Mode PIO Access

Table 13: True IDE Mode PIO Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time (min)	t ₀	600	383	330	180	120	ns
Address valid to -IORD/-IOWR (min) setup	t ₁	70	50	30	30	25	ns
-IORD/-IOWR pulse width 8bit (min)	t ₂	290	290	290	80	70	ns
-IORD/-IOWR recovery time (min)	t _{2i}	—	—	—	70	25	ns
-IOWR data setup (min)	t ₃	60	45	30	30	20	ns
-IOWR data hold (min)	t ₄	30	20	15	10	10	ns
-IORD data setup (min)	t ₅	50	35	20	20	20	ns
-IORD data hold (min)	t ₆	5	5	5	5	5	ns
-IORD data tristate (max)	t _{6z}	30	30	30	30	30	ns
Addresses valid to -IOCS16 assert. (max)	t ₇	90	50	40	N/A	N/A	ns
Address valid to -IOCS16 release	t ₈	60	45	30	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t ₉	20	15	10	10	10	ns

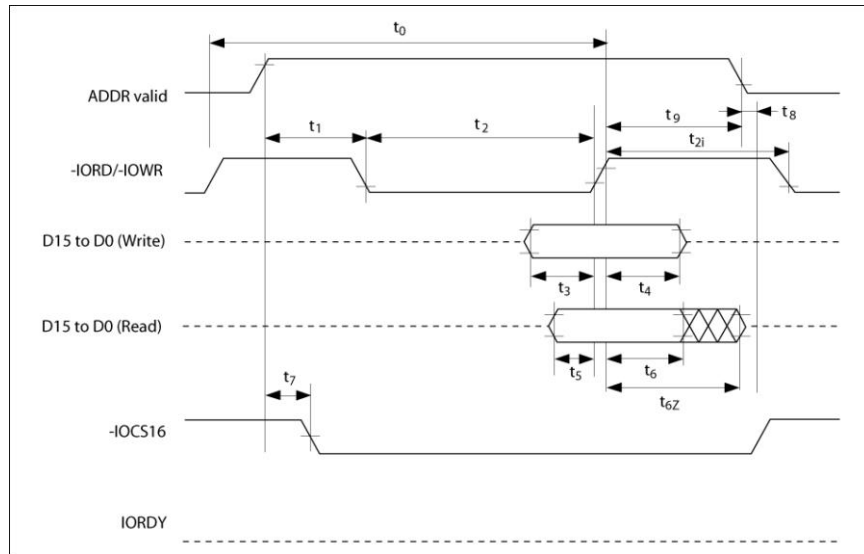


Figure 2: True IDE Mode PIO Access Timing Diagram

3.3.3 True IDE Mode Multiword DMA

Table 14: True IDE Mode Multiword DMA AC Characteristics

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Unit
Cycle time (min)	t_0	480	150	120	ns
-IORD/-IOWR Asserted Pulse (min)	t_D	215	80	70	ns
-IORD data access (max)	t_E	150	60	50	ns
-IORD data hold (min)	t_F	5	5	5	ns
-IORD/-IOWR data setup (min)	t_G	100	30	20	ns
-IOWR data hold (min)	t_H	20	15	10	ns
DMACK to -IORD/-IOWR setup (min)	t_I	0	0	0	ns
-IORD/-IOWR to DMACK hold (min)	t_J	20	5	5	ns
-IORD negated pulse width (max)	t_{KR}	50	50	25	ns
-IOWR negated pulse width (min)	t_{KW}	215	50	25	ns
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	ns
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	ns

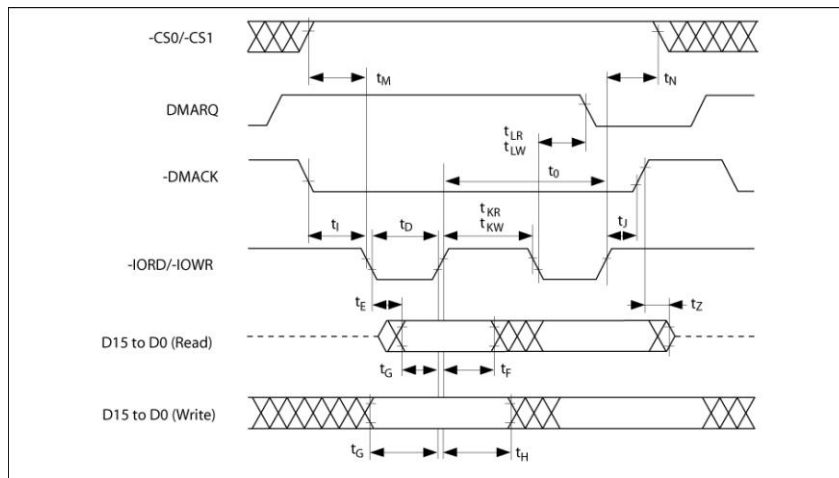


Figure 3: True IDE Mode Multiword DMA Timing Diagram

3.3.4 Ultra DMA AC Characteristics

Table 15: UDMA Burst Timing Requirements

Symbol	UDMA0 (ns)	UDMA1 (ns)	UDMA2 (ns)	UDMA3 (ns)	UDMA4 (ns)	UDMA5 (ns)	UDMA6 (ns)	Measure location (see Note2)
t2CYCTYP (min)	240	160	120	90	60	40	30	Sender
tCYC (min)	112	73	54	39	25	16.8	13.0	Note3
t2CYC (min)	230	153	115	86	57	38	29	Sender
tDS (min)	15.0	10.0	7.0	7.0	5.0	4.0	2.6	Recip'nt
tDH (min)	5.0	5.0	5.0	5.0	5.0	4.6	3.5	Recip'nt
tDVS (min)	70.0	48.0	31.0	20.0	6.7	4.8	4.0	Sender
tDVH (min)	6.2	6.2	6.2	6.2	6.2	4.8	4.0	Sender
tCS (min)	15.0	10.0	7.0	7.0	5.0	5.0	5.0	Device
tCH (min)	5.0	5.0	5.0	5.0	5.0	5.0	5.0	Device
tCVS (min)	70.0	48.0	31.0	20.0	6.7	10.0	10.0	Host
tCVH (min)	6.2	6.2	6.2	6.2	6.2	10.0	10.0	Host
tZFS (min)	0	0	0	0	0	35	25	Device
tDZFS (min)	70.0	48.0	31.0	20.0	6.7	25	17.5	Sender
tFS (max)	230	200	170	130	120	90	80	Device
tLI (min)	0	0	0	0	0	0	0	Note4
tLI (max)	150	150	150	100	100	75	60	Note4
tMLI (min)	20	20	20	20	20	20	20	Host
tUI (min)	0	0	0	0	0	0	0	Host
tAZ (max)	10	10	10	10	10	10	10	Note5
tZAH (min)	20	20	20	20	20	20	20	Host
tZAD (min)	0	0	0	0	0	0	0	Device
tENV (min)	20	20	20	20	20	20	20	Host
tENV (max)	70	70	70	55	55	50	50	Host
tRFS (max)	75	70	60	60	60	50	50	Sender
tRP (min)	160	125	100	100	100	85	85	Recip'nt
tIORDYZ (max)	20	20	20	20	20	20	20	Device
tZIORDY (min)	0	0	0	0	0	0	0	Device
tACK (min)	20	20	20	20	20	20	20	Host
tSS (min)	50	50	50	50	50	50	50	Sender

Notes:

1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.
3. The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4. The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
5. The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

Table 16: UDMA Timing Parameter Descriptions

Symbol	Parameter
t2CYCTYP	Typical sustained average two cycle time
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
tDS	Data setup time at recipient (from data valid until STROBE edge)
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)
tDVS	Data valid setup time at sender (from data valid until STROBE edge)
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)
tCS	CRC word setup time at device
tCH	CRC word hold time device
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.
tDZFS	Time from data output released-to-driving until the first transition of critical timing.
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
tLI	Limited interlock time
tMLI	Interlock time with minimum
tUI	Unlimited interlock time
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)
tZAH	Minimum delay time required for output
tZAD	Drivers to assert or negate (from released)
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)
tIORDYZ	Maximum time before releasing IORDY
tZIORDY	Minimum time before driving IORDY
tACK	Setup and hold times for -DMACK (before assertion or negation)
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

Table 17: Ultra DMA Sender and Recipient IC Timing Requirements

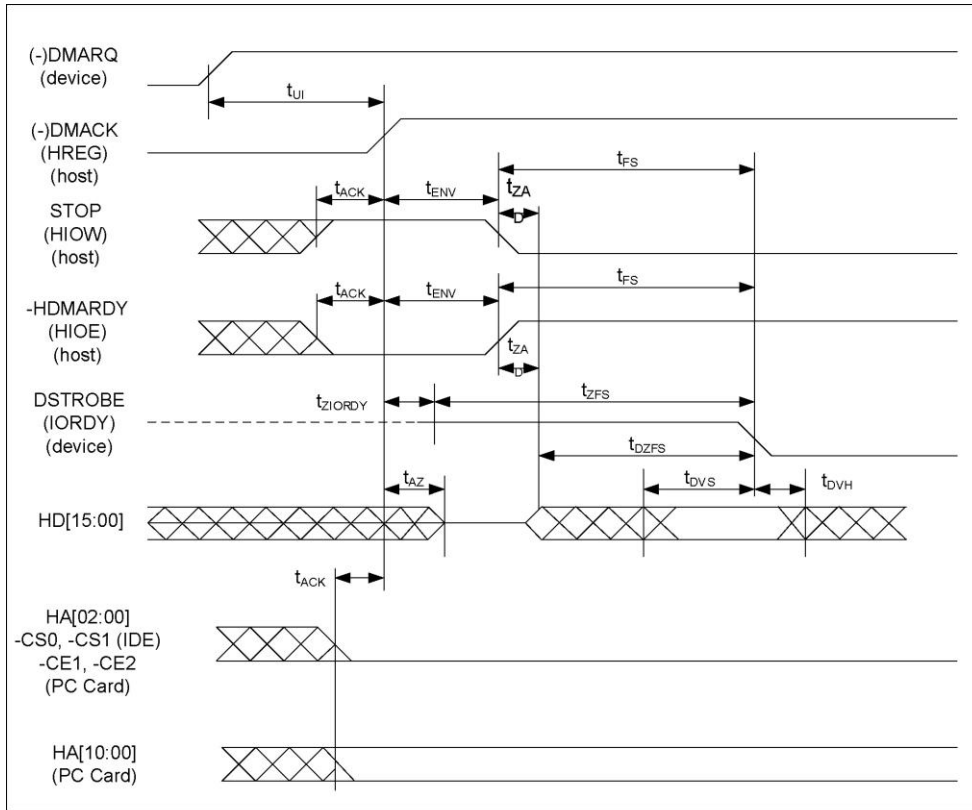
Symbol	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	UDMA6	Unit
tDSIC (min)	14.7	9.7	6.8	6.8	4.8	2.3	2.3	ns
tDHIC (min)	4.8	4.8	4.8	4.8	4.8	2.8	2.8	ns
tDVSIC (min)	72.9	50.9	33.9	22.6	9.5	6.0	5.2	ns
tDVHIC (min)	9.0	9.0	9.0	9.0	9.0	6.0	5.2	ns

Table 18: Ultra DMA Sender and Recipient IC Timing Parameter Descriptions

Symbol	Parameter
tDSIC	Recipient IC data setup time (from data valid until STROBE edge)
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid)
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge)
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid)

Table 19: Ultra DMA AC Signal Requirements

Symbol	Parameter	Max (V/ns)
SRISE	Rising Edge Slew Rate for any signal	1.25
SFALL	Falling Edge Slew Rate for any signal	1.25



Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 4: UDMA Data-In Burst Initiation Timing

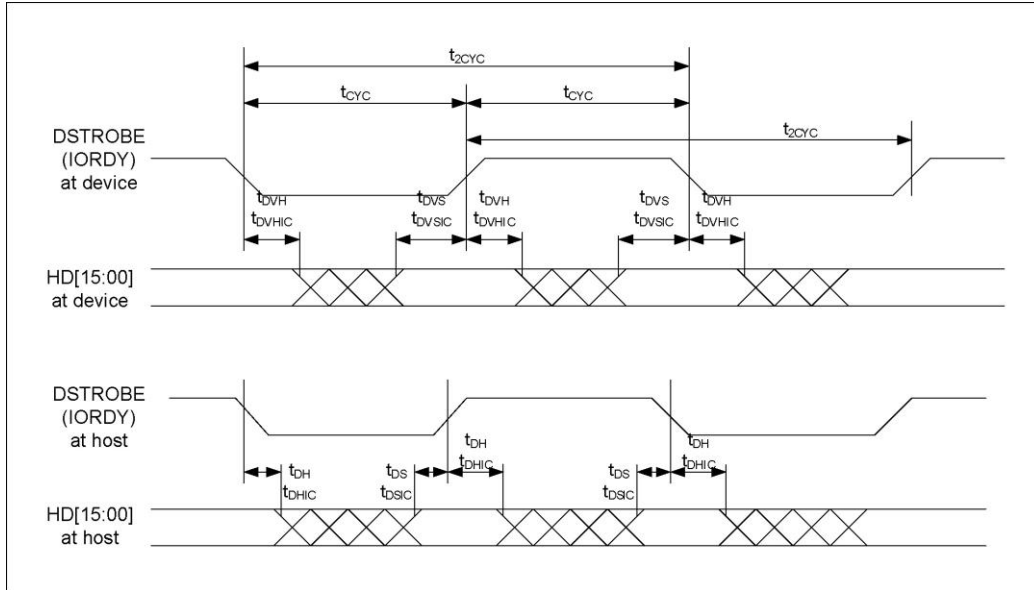
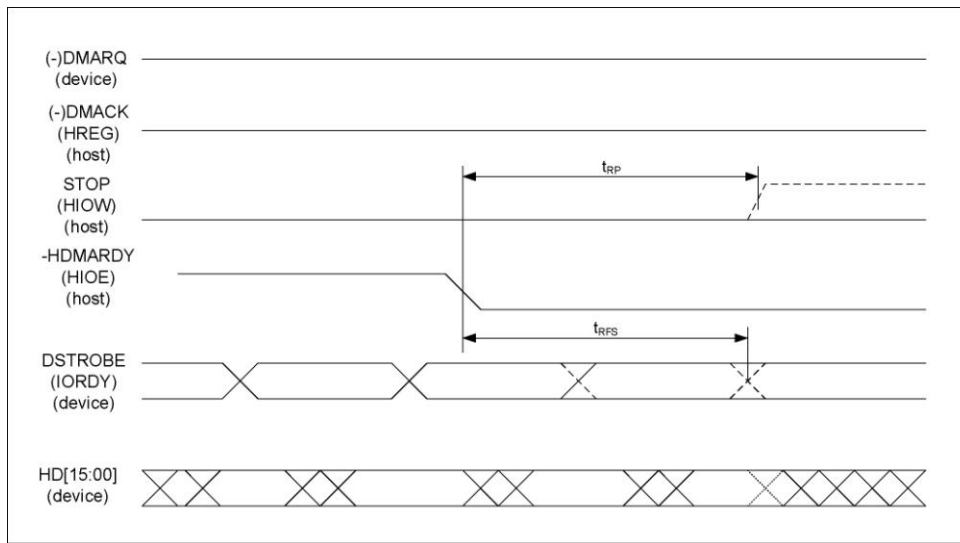
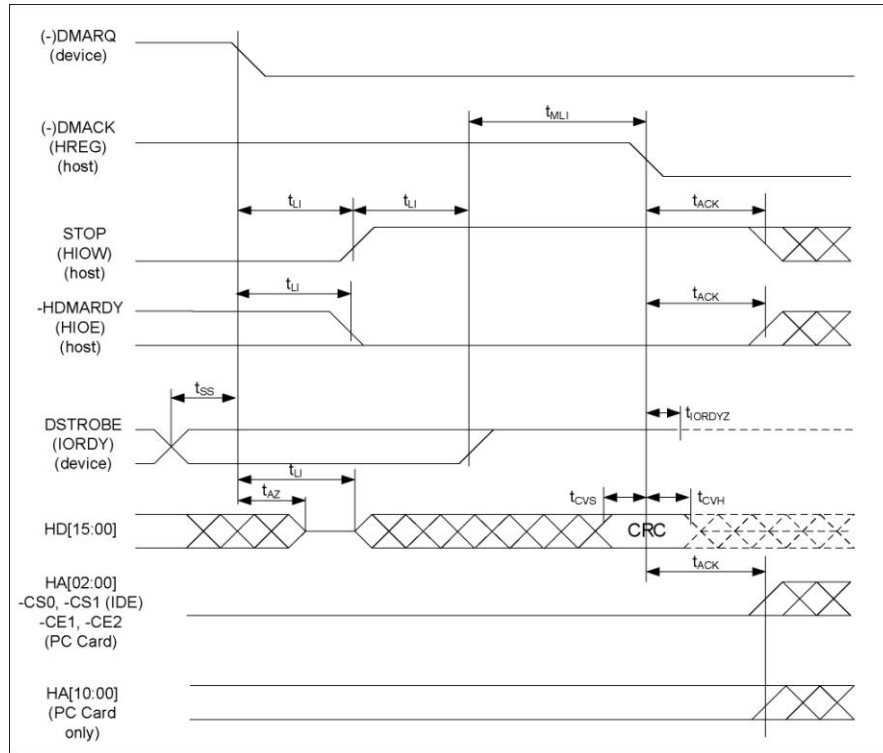


Figure 5: Sustained UDMA Data-In Burst Timing



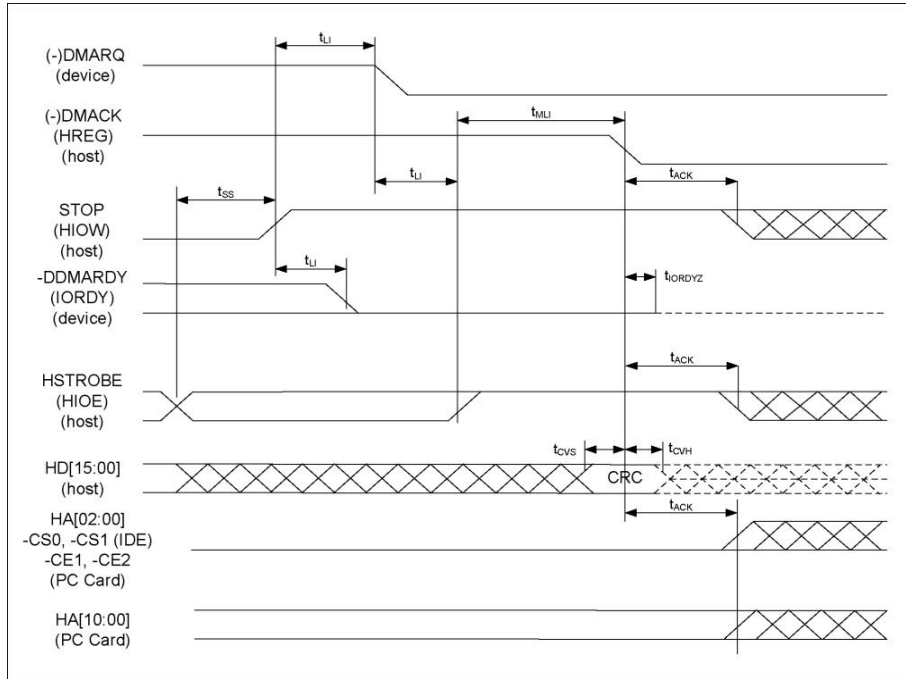
Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 6: UDMA Data-In Burst Host Pause Timing



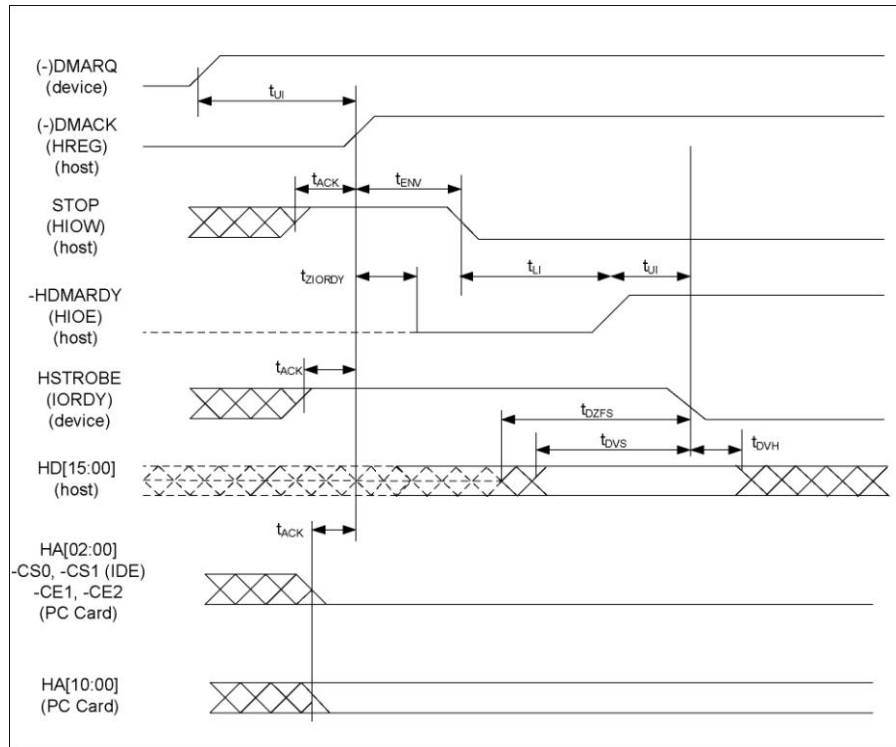
Note: All waveforms in this diagram are shown with the asserted state high.
 Negative true signals appear inverted on the bus relative to the diagram.

Figure 7: UDMA Data-In Burst Device Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 8: UDMA Data-In Burst Host Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 9: UDMA Data-Out Burst Initiation Timing

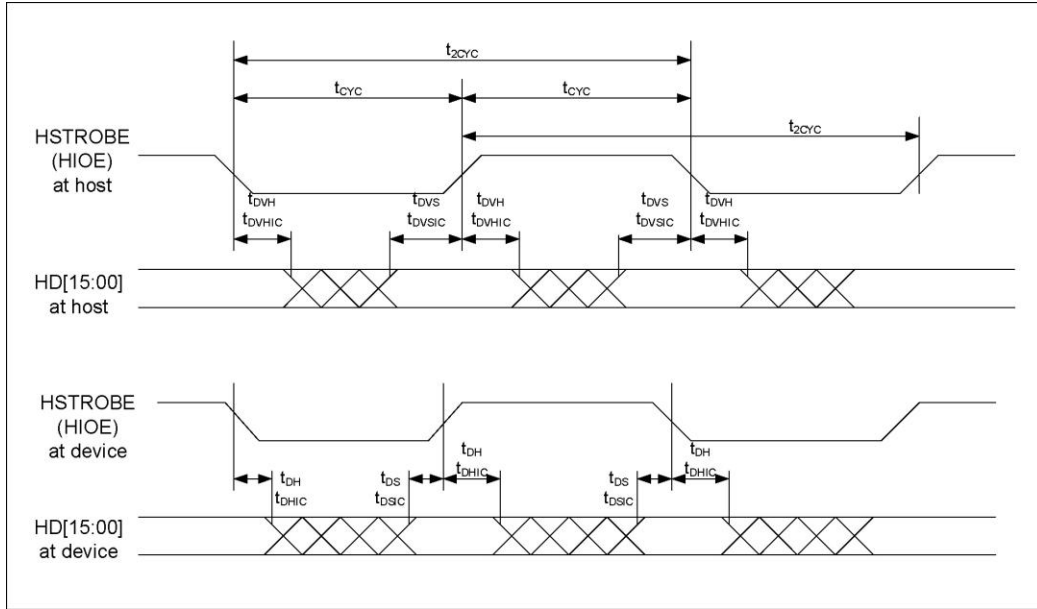
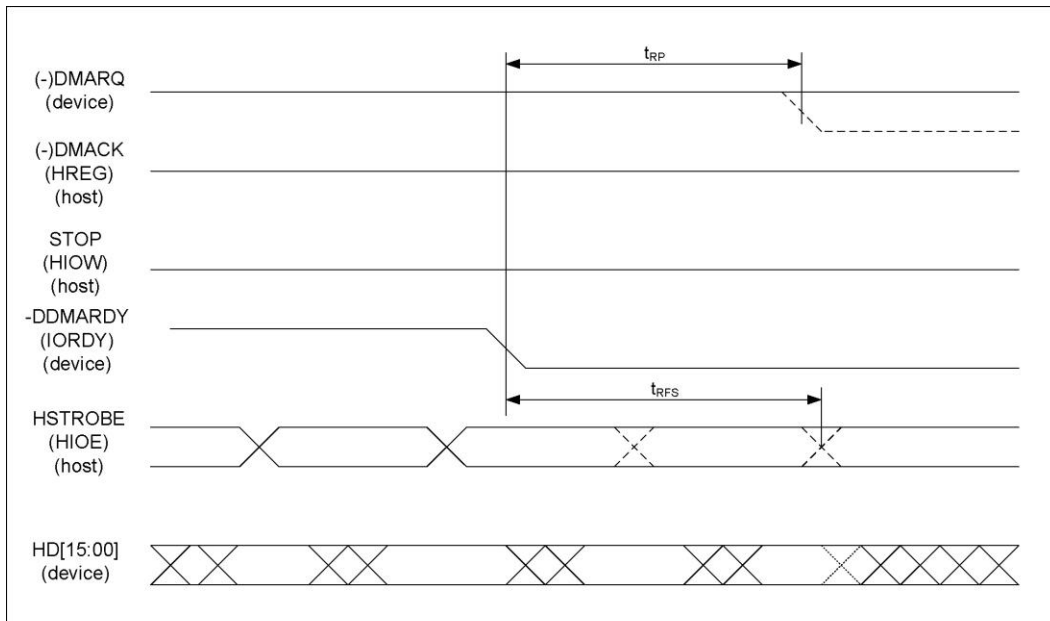
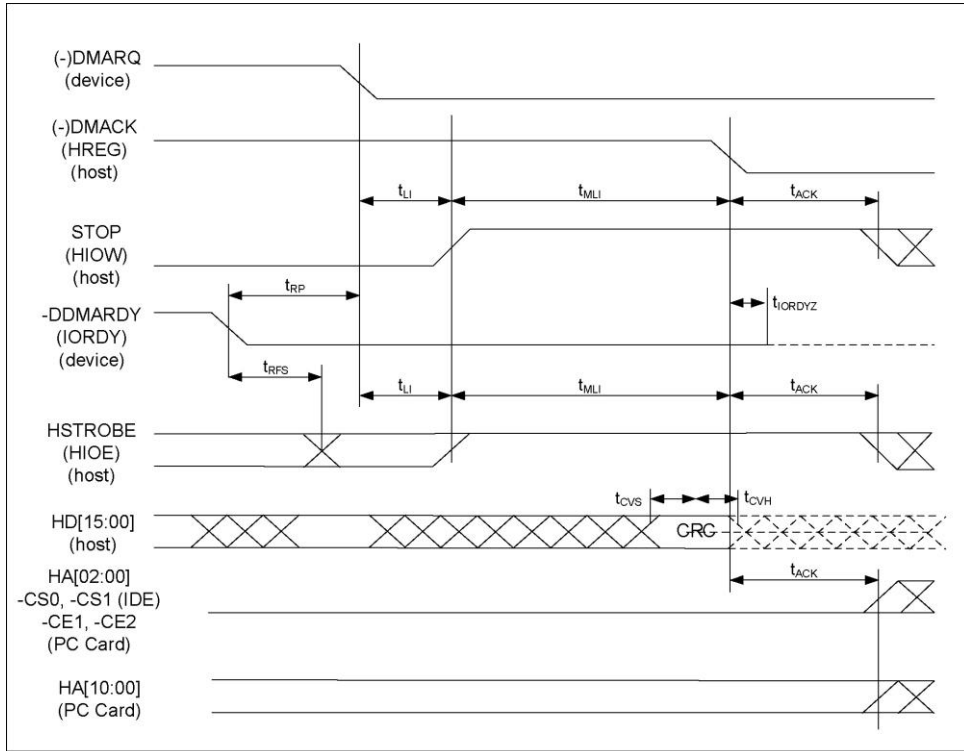


Figure 10: Sustained UDMA Data-Out Burst Timing



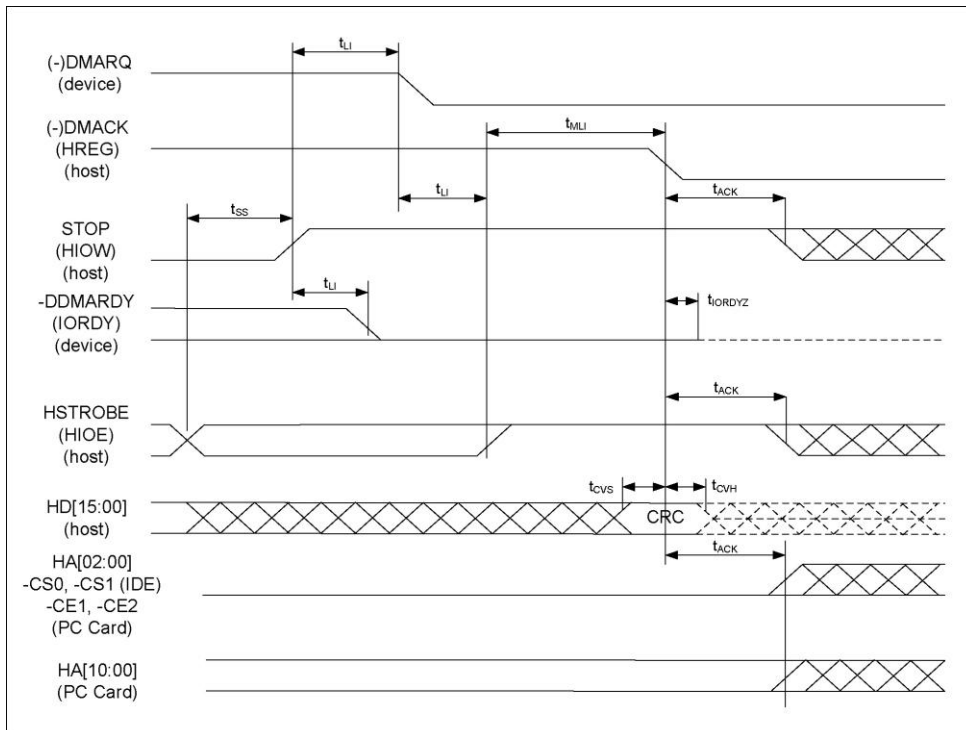
Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 11: UDMA Data-Out Burst Device Pause Timing



Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 12: UDMA Data-Out Burst Device Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Figure 13: UDMA Data-Out Burst Host Termination Timing

Word Address	Data	Total Bytes	Description
55	XXXXH	2	Number of Current Heads
56	XXXXH	2	Number of Current Sectors Per Track
57	XXXXH	2	LSW of the Current Capacity in Sectors
58	XXXXH	2	MSW of the Current Capacity in Sectors
59	010XH	2	Current Setting for Block Count=1 for R/W Multiple commands
60 - 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not supported
63	0007H	2	Multiword DMA modes 0-2 supported
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum multiword DMA transfer cycle time per word (120ns)
66	0078H	2	Recommended multiword DMA transfer cycle time per word (120ns)
67	0078H	2	Minimum PIO transfer without flow control (120ns)
68	0078H	2	Minimum PIO transfer with IORDY flow control (120ns)
69 - 79	0000H	22	Reserved
80	0070H	2	Major revision number; ATA/ATAPI-4 and ATA/ATAPI-5 supported
81-87	XXXXH	2	For bit values indicating supported SMART Features, Refer to 7.1 <i>SMART Support and Identify Command</i> .
88	003FH	2	Ultra DMA modes 0-5 supported
89-255	334	334	Reserved
XXXXH = These values depend on the specific card.			

5.0 Task File Registers

This chapter lists the registers of the mPCI-Express IDE Card. Refer to ATA standards for further details.

Table 21: mPCI-Express IDE Card Task File Registers

Task File Register	Description
Data Register	The Data Register is a 16-bit read/write register used for transferring data between the card and the host. This register can be accessed in word mode and byte mode.
Error Register	The Error Register is a read-only register that is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to "0" (Ready). Diagnostic Codes are returned in the Error Register after a Execute Drive Diagnostic command (code 90h). Extended Error Codes returned in the Error Register after a Request Sense command (code 03h).
Sector Count Register	This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in the register is 0, a count of 256 sectors is indicated.
Sector Number Register	When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.
Cylinder Low Register	In CHS mode (LBA=0), this register contains the low-order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.
Cylinder High Register	In CHS mode (LBA=0), this register contains the high-order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.
Drive/Head Register	This register selects the card's address translation (CHS or LBA) and provides head address (CHS) or high-order address bits 27:24 for LBA.
Status Register	This read-only register indicates status of a command execution. When the BSY bit is "0", the other bits are valid; when the BSY bit is "1", the other bits are not valid. When the register is read, the interrupt pin is cleared.
Alternate Status Register	This register is the same as the Status register, except that is not negated when the register is read.
Device Control Register	This write-only register is used for controlling the interrupt request and issuing an ATA soft reset to the card.
Drive Address Register	This read-only register is used for confirming the card's status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host's I/O space because of potential conflicts on bit 7.
Command Register	This write-only register is used for writing the command that executes the card's operation. The command code is written in the command register after its parameters are written in the Task File during the card's ready state.

6.0 Supported ATA Commands

The ATA commands used by the mPCI-Express IDE Card are listed in Table 22. Refer to ATA standards for details.

Table 22: mPCI-Express IDE Card Supported ATA Commands

Command Set	Code	Description
Check Power Mode	E5h or 98h	This command checks the power mode.
Execute Drive Diagnostic	90h	Command performs internal diagnostic tests implemented by the card. Diagnostic Code is returned in Error Register.
Erase Sector(s)	C0h	Cmd is used to pre-erase/condition data sectors in advance.
Format Track	50h	This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically 00h or FFh). Card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.
Identify Drive	ECh	This command lets the host receive parameter information from the card in the same protocol as Read Sector(s) command.
Idle	E3h or 97h	Command causes the card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
Idle Immediate	E1h or 95h	This command causes the card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt.
Initialize Drive Parameters	91h	This command enables the host to set the number of sectors per track and the number of heads per cylinder.
NOP	00h	No Operation.
Read Buffer	E4h	Command enables host to read contents of card's sector buffer.
Read DMA	C8h	If UDMA is enabled, this command is the sector read command used for UDMA transfer. If UDMA is not enabled, this command is the sector read command used for MWDMA transfer
Read Multiple	C4h	This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Read Long Sector	22h or 23h	Command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
Read Sector(s)	20h (w/ retry) 21h (w/o retry)	Command reads from 1 to 256 sectors as specified in Sector Count register. A sector count of 0 requests 256 sectors. Transfer begins at sector specified in Sector Number register.
Read Verify Sector(s)	40h (w/ retry)	This command verifies one or more sectors on the card by

Command Set	Code	Description
	41h (w/o retry)	transferring data from the flash media to the data buffer in the card and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
Recalibrate	1Xh	The card performs only the interface timing and register operations. When this command is issued, the card sets BSY and waits for an appropriate length of time, after which it clears BSY and issues an interrupt. When this command ends normally, the card is initialized.
Request Sense (Extended Error)	03h	Command requests extended error code after command ends with error. Extended error code is returned in Error Register.
Seek	7Xh	This command is effectively a NOP command to the card although it does perform a range check.
Set Features	EFh	Command is used by the host to establish or select features.
Set Multiple Mode	C6h	Command enables card to perform multiple read and write operations and establishes block count for these commands.
Set Sleep Mode	E6h or 99h	This is the only command that allows the host to set the card into Sleep mode. When the card is set to sleep mode, the card clears the BSY line and issues an interrupt. The card enters sleep mode and the only method to make the card active again (back to normal operation) is by performing a hardware reset or a software reset.
Stand By	E2h or 96h	This command sets the card in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the card returns to the idle mode, the timer starts a countdown. Time is set in Sector Count Register.
Stand By Immediate	E0h or 94h	This command causes the card to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
Translate Sector	87h	This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.
Wear Level	F5h	Command is effectively NOP command and only implemented for backward compatibility. Sector Count Register is always returned with 00h indicating Wear Level is not needed.
Write Buffer	E8h	This command enables the host to overwrite the contents of the card's sector buffer with any data pattern desired.
Write DMA	CAh	If UDMA is enabled, command is the sector write command used for UDMA transfer. If UDMA is not enabled, command is the sector write command used for MWDMA transfer.
Write Long Sector	32h or 33h	Command is provided for compatibility and is similar to Write Sector(s) except that it writes 516 bytes instead of 512 bytes.
Write Multiple	C5h	Command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on transfer of block which contains number of sectors defined by Set Multiple command.

Command Set	Code	Description
Write Multiple w/o Erase	CDh	This command is similar to the Write Multiple command, except that an implied erase before the write operation is not performed. Note: Before using this command, it is required to erase the respective sectors using the Erase Sectors command
Write Sector(s)	30h (w/ retry) 31h (w/o retry)	This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
Write Sector(s) w/o Erase	38h	This command is similar to the Write Sector(s) command, except that an implied erase before the write operation is not performed. Note: Before using this command, it is required to erase the respective sectors using the Erase Sectors command.
Write Verify	3Ch	This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

7.0 SMART Feature Set

Self-Monitoring, Analysis, and Reporting Technology (the SMART feature set) is used to protect the user from unscheduled downtime. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Informing the host system of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action.

7.1 SMART Support and Identify Command

Support for the SMART feature set is indicated by the Identify Command response as follows:

- • Word 82 bit 0 - the SMART feature set is supported.
- • Word 84 bit 1 – SMART self test supported
- • Word 84 bit 0 – SMART error logging supported

Enabled indicators for the SMART feature set are as follows:

- • Word 85 bit 0 - the SMART feature set has been enabled
- • Word 87 bit 1 – a 1 indicates that SMART self test is enabled (default)
- • Word 87 bit 0 – a 1 indicates that SMART error logging is enabled (default)

7.2 SMART Commands

A command code of 0xB0 with a SMART command selected in the Feature Register invokes a SMART command. Refer to Table 23 for the Feature Register values associated with each SMART command.

Table 23: Supported SMART Commands

Feature Register	Command	Note
D0h	SMART READ ATTRIBUTE DATA	Optional - supported
D1h	SMART READ ATTRIBUTE THRESHOLDS	OBS – supported
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	Mandatory
D3h	SMART SAVE ATTRIBUTE VALUES	OBS – supported
D4h	SMART EXECUTE OFF-LINE IMMEDIATE	Optional - supported
D5h	SMART READ LOG	Optional - supported
D6h	SMART WRITE LOG	Optional - supported
D8h	SMART ENABLE OPERATIONS	Mandatory
D9h	SMART DISABLE OPERATIONS	Mandatory
DAh	SMART RETURN STATUS	Mandatory
DBh	SMART Enable/Disable Automatic Off-line	OBS – supported

7.3 SMART Attributes

The SMART attributes used by the card are listed in Table 24.

Table 24: mPCI-Express IDE Card Supported SMART Attributes

ID	Name	Description	Type
1	Raw Read Error	Count of raw data errors while data from media, including retry errors or data error (uncorrectable)	Warranty
2	Throughput Performance	Internally measured average and worst data transfer rate	Warranty
5	Reallocated Sector Count	Count of reallocated blocks. In the case of the mPCI-Express IDE Card, this will be count of reallocated or remapped blocks during normal operation from the grown defect table	Warranty
9	Power On Hours	Number of hours elapsed in the Power-On state	Advisory
12	Power Cycle	Number of power-on events	Advisory
13	Soft Read Error Rate	Number of corrected read errors reported to the operating system (SLC = 3 or more bits; MLC =5 or more bits)	Advisory
100	Erase/program cycles	Count of erase program cycles for entire card	Advisory
103	Translation Table Rebuild	Power backup fault or internal error resulting in loss of system unit tables	Advisory
170	Reserved Block Count	Number of reserved spares for bad block handling	Warranty
171	Program Fail Count	Count of flash program failures	Advisory
172	Erase Fail Count	Count of flash erase command failures	Advisory
173	Wear Leveling Count	Worst case erase count	Advisory
174	Unexpected Power Loss	Attribute counts number of unexpected power loss events	Advisory
184	End-to-end error detection	Tracks the number of end to end internal card data path errors that were detected	Warranty
187	Reported Uncorrectable Errors	Number of uncorrectable errors reported at the interface.	Advisory
188	Command Timeout	Tracks the number of command time outs as defined by an active command being interrupted	Advisory
194	Temperature	Temperature of the base casting.	Advisory
196	Reallocation Event	Total number of remapping events during normal operation and offline surface scanning.	Advisory
198	Offline Surface Scan	# of uncorrected errors that occurred during offline scan.	Advisory
199	UDMA CRC Error	Number of CRC errors during UDMA mode	Advisory

8.0 Revision History

Revision	Date	Description
-101	5/12/08	Initial release.
-102	5/29/08	# of LBA and Cylinders updated in CHS Parameters table.
-103	6/2/08	General Description updated.
-104	6/13/08	ICC, ICC(SB), and ICC(Idle) typical currents added.

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